

SCIENTIFIC DATA SYSTEMS

SDS T SERIES

Integrated Circuit Logic Modules Description and Specifications

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SDS T SERIES Integrated Circuit Logic Modules

Description and Specifications



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PRODUCT INDEX

Inside Back Cover

Output Loading: Buffer amplifier, inverter amplifier, or flip-flop can drive 14 unit loads.

When amplifier outputs are wired together to form gating functions (see page 13), each additional output attached to the first one applies 2 unit loads but does not add drive capability. (In the worst case, only one amplifier is conducting).

<u>Timing</u>	<u>Typical</u>	<u>Worst-Case</u>
Propagation Delay: AND/OR (Buffered) or NAND/NOR (Buffered):		
Flip-flop:	18 nsec.	30 nsec.
	40 nsec.	60 nsec.

Frequency Range (Clock Frequency): d-c to 10 Mc

Minimum Input Timing Requirements (Typical): Flip-flop d-c input (mark or erase) must be true for at least 40 nanoseconds.

Flip-flop a-c input (set or reset) must be true for 30 nsec. before clock changes from true to false, 5 nsec. thereafter.

Minimum Clock Duration for Flip-Flop: Clock true for 30 nanoseconds, clock false for 60 nanoseconds.

Temperature

Full-Performance Ambient Operating Temperature: 5°C to 71°C (41°F to 160°F)

Storage Temperature Range: -55°C to +150°C

MECHANICAL

Card Size & Type

4-1/4 inches by 4-3/4 inches, epoxy-glass, etched copper wiring.

Connectors

52 gold-plated contacts mating with spring-loaded bifurcated (dual prong) connectors. Contacts are 0.15 inches apart; cards are spaced 0.50 inches center to center. Keyed connectors prevent wrong insertion.

Back Panel, Wiring

Terminations for wire-wrap, solderless push-on, or solder tail connection feed through epoxy-glass back panel which is covered with etched copper ground plane for high frequency shielding. Four terminals from each card position are soldered to ground plane. Power connections are on etched circuit back panel and are connected to appropriate connector pin terminations.

Recommended Wire: No. 28 AWG copper with polyethylene insulation.

Mounting Cases

19 inches wide by 5-1/4 inches high, fixed or hinged (32 cards); or 90 card pull-out drawer, 19 inches by 8-3/4

inches. Welded all steel cases with ventilation slots, multiposition mounting hardware, and optional blowers.

HOW T SERIES MEETS SYSTEM REQUIREMENTS

SYSTEM DESIGN GOALS

Good system design demands high performance at low cost.

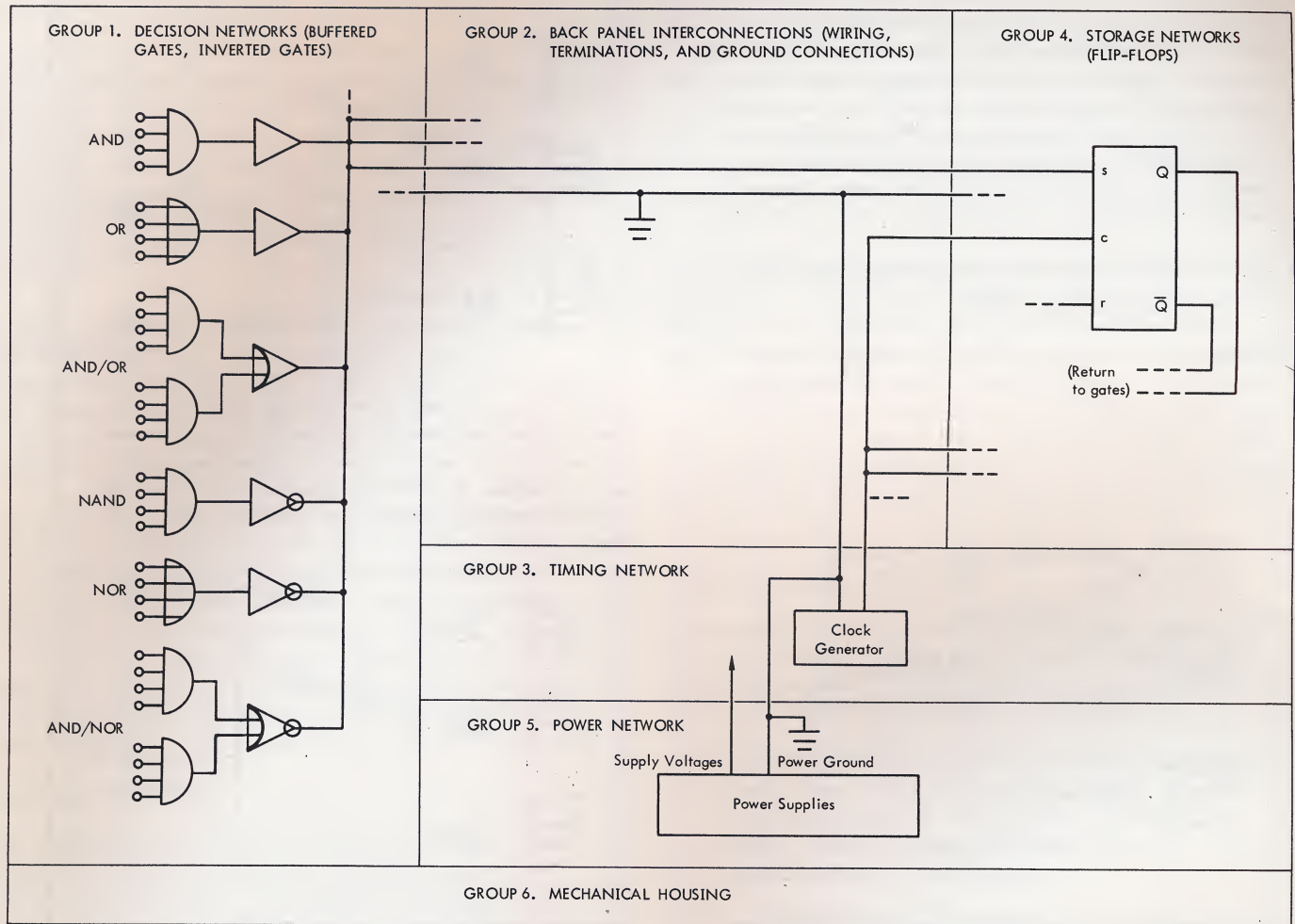
In many digital applications, prime PERFORMANCE goals are:

1. Eliminate error (erroneous triggering)
 - a. Minimize noise generation or pickup and reject noise at logic inputs
 - b. Maintain accurate timing
 - c. Restore attenuated signals to retain signal integrity
2. Achieve fast system speed
 - a. Achieve fast rise and fall times on logic level changes
 - b. Minimize propagation delays in logic circuits and wiring
 - c. Minimize sum of delays in series in each logic chain

The corresponding ECONOMIC goals are:

1. Minimize engineering and related technical labor
 - a. Mechanize logic equations simply, rapidly
 - b. Plan interconnections quickly
 - c. Avoid design of special circuits
 - d. Assemble system quickly, conveniently
 - e. Debug system quickly
 - f. Eliminate callbacks to correct failures
2. Minimize hardware cost
 - a. Minimize number of logic elements for given logic function
 - b. Minimize cost per element
 - c. Minimize cabinet hardware required (achieve dense packing)
 - d. Minimize cost of other accessories (power supplies, etc.)
 - e. Minimize replacement part quantities
3. Minimize equipment failure
 - a. Avoid inconvenient or costly disruption of system operation
 - b. Eliminate troubleshooting and replacement costs

These goals can be translated into specific hardware design goals. Hardware can be lumped into six broad classes for this analysis (see diagram below). Each group has its own performance and economic demands, and each will be described in sequence.



GROUP 1. DECISION NETWORKS

Design of gate networks, usually with the aid of Boolean algebra, is often the most time-consuming task. In many cases gates and amplifiers also constitute the bulk of the system hardware. Thus, for economy, standard gate-amplifier configurations should be designed to: 1) minimize implementation time, 2) minimize the total number of gates and amplifiers in the system, and 3) cost less per gate or amplifier unit.

Minimize Implementation Time

The best way to minimize implementation time is to make all four logic functions, AND, OR, NAND, and NOR, available to the designer at the same low cost. T Series does just this. The principle is called natural logic. Once the Boolean expressions that define a logic function have been reduced to simplified form the mechanization task is almost finished. The designer then substitutes T Series gating structures directly for equation terms (see Example I).

Many manufacturers urge the exclusive use of NAND or NOR functions. They standardize on one inverting gate type to solve their problems rather than the user's. Implementation only with NAND or NOR functions requires additional equation manipulation. T Series eliminates the extra design work by economically providing all four functions. A combination of standardized integrated amplifier circuits with flexible discrete diode-resistor gates, unique with SDS, makes this possible.

Logic element modules contain a calculated mix of gate combinations with gates having from 2 to 5 inputs. This selection permits the designer to choose the right combinations of circuits from each card, reducing leftover circuits in the rack and avoiding many wiring problems. The 52 connectors per card permit full access to each circuit.

Load calculations are simple. All T Series logic elements are rated in unit loads of 3.8 ma. Each diode gate always places 1 unit load on the previous amplifier output.

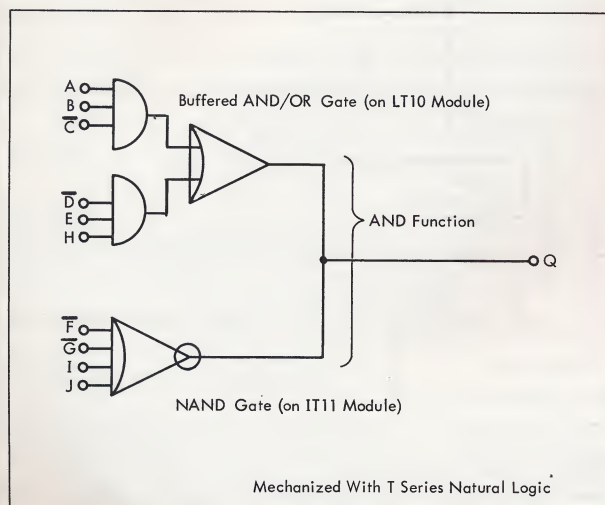
EXAMPLE 1 - NATURAL LOGIC IMPROVES PERFORMANCE AND COSTS LESS

The monolithic integrated buffers, inverters, and flip-flops of T Series are designed to accept inputs from diode AND and OR structures. The unique SDS gating and buffer designs permit three stages of logic to be performed with a single stage of amplification. Any active element such as a non-inverting amplifier may have AND/OR input gates (two stages) and also may have its outputs paralleled with other active element outputs to implement a third stage.

As an example, mechanize the following function:

$$Q = (ABC + DEH) (\overline{FGIJ})$$

T Series natural logic permits direct substitution of hardware for equation terms, as shown below. Note that only two amplifiers are required, one a buffer and one an inverter (NAND).

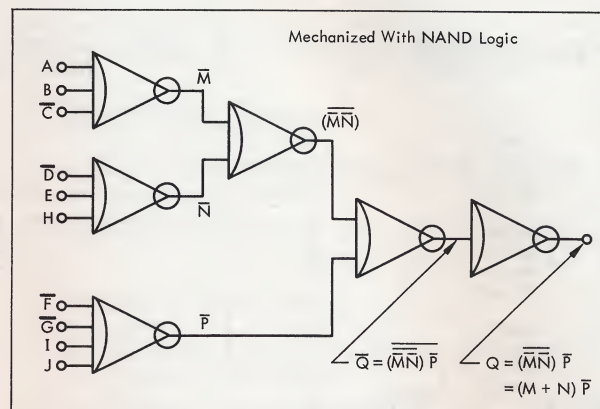


NAND functions are the most commonly available monolithic gate structures offered by other manufacturers. Implementation using NAND functions alone (without forming AND gates by connecting amplifier outputs) is much more complex. First, the equation must be manipulated to represent a series of not-AND operations, of the form $Q = \overline{Y \cdot Z}$, where $Y = \overline{V \cdot X}$, $Z = \overline{T \cdot U}$, etc. Let $M = ABC$, $N = DEH$, and $P = \overline{FGIJ}$. By DeMorgan's theorem, the original expression may be rewritten

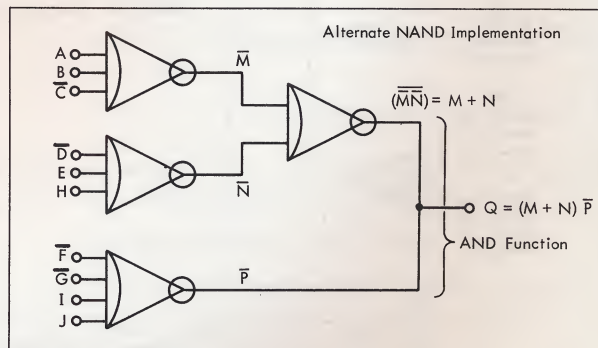
$$Q = (M + N) \overline{P} = (\overline{\overline{M} \overline{N}}) \overline{P},$$

which puts it in the proper form for NAND implementation, providing one more inverter is added since the last NAND gate results in an inversion.

The structure that results using NAND gates is shown in the next column. Note that it uses 6 amplifiers as compared with 2 for the natural logic version.



Mechanizing the same function with NOR gates is similar, but requires 5 amplifiers if all complements are available, 7 amplifiers if only the given signals are available. If ANDing at outputs is allowed the implementation is simpler, but still requires 4 amplifiers:



For a cost comparison, if we assume that each buffered logic function sells for roughly the same price, then the T Series approach costs 1/2 as much as the best NAND implementation, in this typical example.

To facilitate a comparison of relative delay times, assume that D is the average propagation delay of a diode AND gate or a diode OR gate. Then 5D is a realistic approximation of the delay of an inverting or a non-inverting amplifier. To favor NAND logic, further assume that 5D is also the delay of a monolithic NAND structure. The resulting total delay for the typical circuit illustrated above is 7D with SDS T Series, 20D with straight NAND logic, and 10D with NANDs ANDed at the output.

This example shows dramatically how one powerful feature of T Series becomes apparent in a system application. Comparison with other module lines on an individual circuit for circuit basis reveals only part of the full merit of T Series modules.

Minimize Hardware Quantity

The number of gates and amplifiers required to implement a given gating function must be the lowest possible.

Amplifiers in particular should be minimized, since they are the active (and therefore expensive) components. Primarily they furnish power to drive logic signals through the gating structure. They also can perform logical inversion, if required. Where adequate power is available and amplifiers are used merely to perform logic inversions not required by the most simplified form of the equations, they are an inexcusable expense. Example 1 explains how they may be eliminated.

Example 1 also demonstrates another T Series feature that eliminates amplifiers. This is the ability to perform 3 stages of logic (AND-OR-AND) with 1 stage of amplification, without loss of signal quality. The combination of the unique AND/OR gate, with AND functions formed at amplifier outputs, makes this possible.

The number of amplifiers is also cut by making output driving current high; this permits each amplifier to drive more gates. The fan-out from an SDS buffer or inverter amplifier is 14 unit loads (compared to 8 for many other makes of integrated circuit modules).

These three T Series features (natural logic, 3 levels, high fan-out) typically yield hardware savings of at least 1/3 when compared to other module lines.

Minimize Circuit Costs

SDS achieves low unit circuit costs by integrating the repetitive clusters of components that occur mainly in amplifiers and flip-flops. The number of different integrated circuit types is kept small to simplify design and manufacturing. By retaining the inexpensive gate structure outside the integrated circuit, T Series retains the flexibility of natural logic. Logic modules (excluding special circuits) use only seven different components: 3 integrated circuit types, 3 resistor types, and 1 diode type. Individual circuit costs are thereby held to a minimum.

GROUP 2. INTERCONNECTIONS

Sources of Digital System Noise

Poorly designed circuits, wiring, or logic can cause unpredictable switching which introduces errors into data. Digital noise is defined as any unwanted voltage change on the two standard logic levels. Noise can be an internally generated short-duration pulse or a long-duration d-c drift. In addition, there can be pickup of external signals, radiated from nearby devices outside the logic network.

High speed digital systems are particularly subject to pulse-type noise because logic levels must change rapidly

to maintain both timing accuracy and system speed. Fast level changes produce high-frequency components which couple readily into the wrong circuits through interwiring capacitance. Noise can also be caused by reflections of leading and trailing edges of pulses. The longer segments of interconnecting wiring act as transmission lines to the high-frequency transient components of logic signals. If these transmission lines are not properly terminated in their characteristic impedances, various reflections can interfere to cause false switching.

The ground system can create its share of problems at high frequencies. If inductive reactance is high, which often happens when large loops are created by using wires as ground returns, sharp noise pulses may occur at circuit input ground connections.

Another possible cause of signal degradation is poor contact mesh at the connectors which link the modules to the back panel wiring. Poor mesh or corrosion can lead to intermittent high resistance in logic signal lines.

Minimize Digital System Noise

These problems can be controlled through proper design of the interconnecting wiring and the ground system, and by establishing adequate noise thresholds at the gates. A number of specific objectives may be stated:

1. Prevent inductive or capacitive coupling among back-panel wires. Also prevent coupling between these wires and sources of noise signals external to the system. Design the ground system to have low inductance as well as low resistance.
2. Design the back-panel interconnections to approximate transmission lines in order to achieve characteristics that are independent of frequency. Then terminate these lines (when long) with resistance close to their characteristic impedance, to reduce pulse reflections.
3. Reduce the possibility of poor contact mesh at connectors.
4. Design the gates to have high immunity to noise.

These design goals are all incorporated in T Series.

First, the ground for each module case is a flat copper sheet attached to an epoxy-glass board that runs the full width and height of the case. It has very low resistance, and the loops formed by the plane and each interconnecting wire have low inductance.

The ground plane is used as a return path for currents in back-panel wires. This has the effects of shielding each conductor from each other conductor and of turning each

conductor into a transmission line. If the back panel wires are pushed down close to the shield plane the approximate characteristic impedance that results is about 150 ohms.

Second, the terminating impedance at the far end of a long back panel logic signal line may be made to approximate line impedance by connecting a standard 220 ohm terminating resistor, greatly reducing the amplitude of signal reflections. This is possible with T Series because the discrete terminating resistors (and gate resistors) are outside the integrated circuit container, and power dissipation therefore is not a limiting factor. Signal reflection problems often arise in systems that rely exclusively on monolithic integrated circuits because the integrated load resistances must be considerably larger than line impedance in order to avoid excessive dissipation within the integrated circuit package.

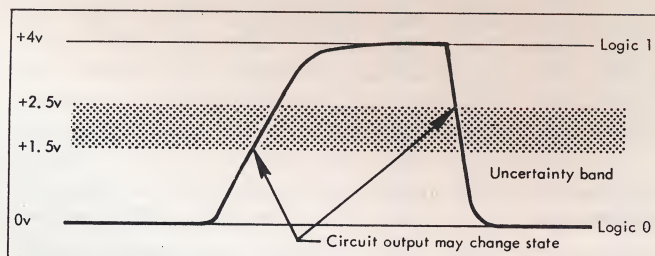
Third, poor contact mesh is eliminated with an exclusive T Series design. The connector receptacles for module edge contacts have one pair of bifurcated (forked conductor), spring loaded, gold plated fingers for each module edge contact. Gold plating reduces the probability of high resistance oxide formation. The fingers are so designed that they cannot distort or lose their spring pressure. Bifurcation provides redundant contacts, further reducing the already remote probability of contact resistance problems. These new connectors are manufactured to SDS specifications and are available only with T Series.

Wires may be attached to the connector pins (which protrude through openings in the ground plane) with reliable wire-wrap, solder tail, or new solderless crimp/push-on terminals.

The preceding describes the various techniques used to reduce noise. However, since some noise is inevitable, the gates must be able to reject it. The gate switching point is therefore placed at +2 volts and the uncertainty band about this value is made as small as possible through tight component tolerance control.

Noise Rejection Specifications

With a signal at 0 volts (logic 0 level), noise on a gate input of up to +1.5 volts will not cause the associated amplifier output to change state. With a signal at +4 volts (logic 1 level), noise on a gate input of -1.5 volts maximum, which brings logic 1 voltage down to +2.5 volts, will not cause the associated amplifier output to change state. This leaves an uncertainty band between +1.5 volts and +2.5 volts, within which the amplifier output will switch.



These thresholds are determined by characteristics of the gate diodes, gate resistors, and the integrated amplifier input circuits. The superior noise rejection properties of T Series stem from close tolerance control.

GROUP 3. SYSTEM TIMING (SPEED)

Propagation Delays and Clock Frequency

Delay is the time required for a signal to propagate through a circuit. In an idealized sense, it is defined as the time lag between arrival of a step function at a circuit input, and the appearance of a resultant step function at its output.

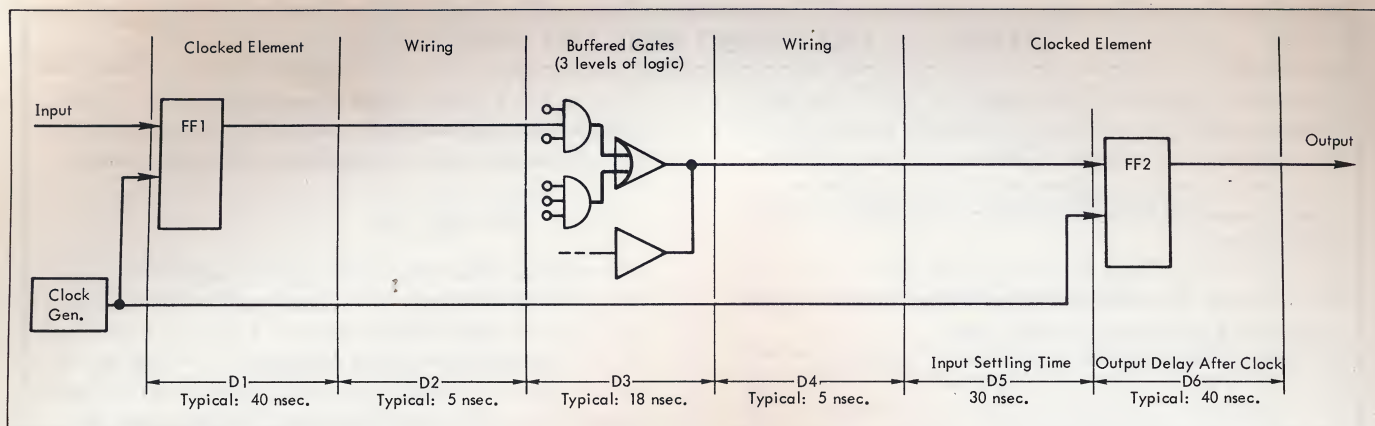
Operating Frequency Range is the repetition rate range of clock pulses over which the clocked system performs reliably in continuous operation while meeting all other specifications.

Since system speed is loop delay limited it makes no sense to emphasize high clock rate by itself as a desirable feature. A clock oscillator may easily be designed to operate at frequencies unheard of in digital work, but this is no guarantee that a system may be operated at that frequency. The clock must operate slowly enough to permit all logic signals to propagate through appropriate gates to the next level of flip-flops before the next clock pulse occurs. In other words, the logic circuits must have time to complete their decisions before the clock commands the flip-flops to store the results and commence the next level of logical decisions.

The diagram, page 7, illustrates these points. Assume the input is true. When a clock falling edge occurs flip-flop F1 is set. Its output changes after internal delay D1. This signal is propagated through a series of wiring paths, gates, and amplifiers with a total delay $D_2 + D_3 + D_4$, until it reaches another clocked element, FF2. Then FF2 may be triggered by a second clock falling edge after a stabilizing period, D5, and the output is available after an internal delay D6. The clock pulse falling edges, which trigger the flip-flops, cannot be allowed to occur at shorter intervals than the total series delay, $D_t = D_1 + D_2 + D_3 + D_4 + D_5$. Thus the maximum permissible clock rate in this example is $1/D_t$. (This has no direct relation to the rate at which a single flip-flop can be toggled).

System design can be varied to some extent to minimize total system delay by performing whole functions in parallel rather than in series. However, the minimum delay in any single chain of elements as illustrated below can only be reduced (and clock rate raised) if:

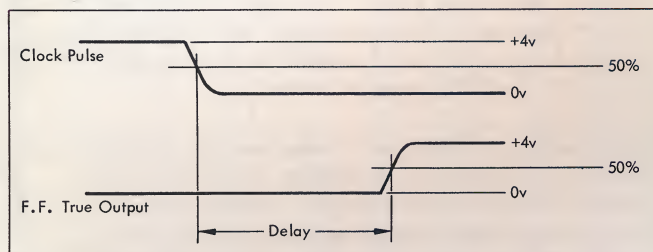
1. Internal delays of flip-flops and amplifiers are minimized
2. Wiring delays are minimized
3. Signal settling time and clock sampling period are minimized



Minimize Active Circuit Delays

The T Series active circuits have very short internal delays. Buffer or inverter amplifiers have delays (with input gates included) of 18 nanoseconds typical, 30 nsec. worst case.

Flip-flop delay is 40 nsec. typical, 60 nsec. worst case, measured as follows:



Minimize Delay Due To Wiring

The internal delays of the active circuits, given above, are measured with the active circuits loaded to permit minimum rise (or fall) time at the output. In actual practice, when the active circuit output is used to drive a load consisting of back panel wiring and gates, the rise (or fall) time is extended. This difference is the delay due to wiring.

The factors which determine delay due to wiring are driver output characteristics, propagation velocity, length of line driven, and load characteristics; length of line and load characteristics are the major contributors to wiring delays. Rise time and fall time are usually slightly different because the driver output presents a high impedance during the 0 to 1 transition, and a low impedance during the 1 to 0 transition.

On the 0 to 1 transition the wiring acts as a capacitive load on the driving circuit; wiring delay depends on how fast this capacitance charges. The capacitive characteristic is due not only to stray capacitance, but also to the fact that each wire, which approximates a 150 ohm transmission line, is always loaded with a resistance somewhat greater than its characteristic impedance of 150 ohms, and therefore behaves as a capacitive load. If terminating

resistance is decreased to more closely match line impedance, the line behaves more like a resistive load, but fan-out is sacrificed.

T Series circuit parameters are chosen for both high fan-out and fast rise times (short delays), as explained in example 2.

In addition the logic designer has at his disposal the means to trade between fan-out and delay to meet higher speed requirements. He can reduce rise time (at the cost of fan-out) by adding a 5 unit load (220 ohm) terminating resistor to the end of a line, decreasing the RC time constant.

On the 1 to 0 transition the wiring acts generally as an inductive load because the internal impedance of the driving transistor in the conducting condition is very low. This delay is generally less than during the 0 to 1 transition.

Typical back-panel wiring delays are 5 to 15 nanoseconds.

Minimize Settling Time

A T Series flip-flop set or reset input must be true for at least 30 nanoseconds before clock changes from true to false and stay true for 5 nanoseconds thereafter.

Conclusion

The example shown at the top of the page is a typical configuration, having three levels of logic (AND/OR/AND) between clocked elements. The total loop delay that may be normally expected under these circumstances is obtained by adding the figures given:

$$D_t = D_1 + D_2 + D_3 + D_4 + D_5 \\ = 40 + 5 + 18 + 5 + 30 = 98 \text{ nanoseconds.}$$

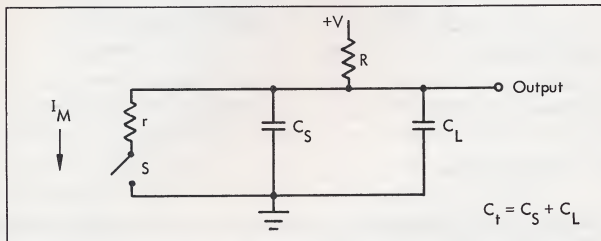
This allows the use of a clock frequency of $1/98 \times 10^{-8} =$ approx. 10 Mc.

As can be seen by comparing T-Series delay times with those of other module types, the circuit internal delays, the per-unit wiring delays, and settling delays are at a minimum. If the design objective is maximum speed, then the real pay-off lies in reducing the number of series amplifiers and the length of wiring. T Series achieves this objective through natural logic.

EXAMPLE 2 - HIGH CURRENT DRIVE AIDS SYSTEM SPEED

Very high current-handling capability of T Series integrated circuits (up to 60 ma.) is directly responsible for two important advantages. One is the exceptionally high fan-out of 14 (compared with about 8 offered by other integrated circuit modules). The other is faster system speed.

Shown below is a first approximation schematic of an integrated circuit driving an RC load.



Switch S and small resistance r roughly represent the output transistor of a monolithic gate or flip-flop. Symbol I_M denotes the maximum current handling ability of the output transistor at the 0 level, or fully "on" condition (S closed). Since r typically is small, load resistance R and supply voltage V must be chosen so that current through the transistor in the steady "on" condition does not exceed the limiting value, I_M . Thus with a given supply voltage, V, and a given maximum current handling capability, I_M , $R = V/I_M$.

C_S represents shunt and parasitic capacitance of the transistor. Load capacitance C_L is wiring and pin capacitance to ground, and depends on the length of line driven and the number of connector pins. The total, $C_T = C_S + C_L$.

If the transistor initially is in the "on" condition, with maximum current I_M , output voltage will be nearly zero.

If the switch is then opened (transistor cut off), output voltage rises exponentially toward V. The rate of output voltage buildup is controlled by the time constant:

$$RC_T = \frac{V}{I_M} C_T.$$

This equation shows that with a given capacitive loading, the rate of change of voltage on the interconnecting wiring in going from 0 level to 1 level is controlled by the load resistance, and therefore is limited by the ratio of supply voltage to transistor output current handling ability. The lower the supply voltage and the higher the current handling ability, the lower the load resistance (R) that can be used, and therefore the faster the rise times when current is turned off. SDS T Series integrated circuits operate with a low supply voltage and have output transistors with very high output current handling ability, to quickly drive the system through logic level changes.

The real test of any circuit is its speed under load. T Series integrated circuits maintain their high operating speed under conditions of capacitive loading that significantly slow less powerful circuits.

This example is simplified to illustrate the principle involved. In practice, as many as 14 gating circuits are connected across the output. During a 0 to 1 level change each conducting gate supplies 1 unit load of charging current through a pull-up resistor connected to +8v. The supply voltages, load resistance, and pull-up resistances all are chosen so that steady-state current through transistor S does not exceed limiting value I_M . The conclusions of a more detailed analysis are the same: the higher the current handling ability, and the lower the voltages used, the faster the capacitive load can be charged.

GROUP 4. STORAGE NETWORKS

A flip-flop should be both versatile and economical. If possible, it should be designed to minimize interconnecting wiring in the majority of applications. It should have high current output to eliminate the need for amplifiers to drive the next stages of gating.

To enhance system performance the flip-flop should have minimum internal delay, for high speed applications. It should also have a short, precisely timed sampling period (time during which it is sensitive to inputs) in order to avoid erroneous triggering. It must also be insensitive to temperature variations and have excellent long term stability, to prevent erroneous switching due to change in circuit characteristics. Level changes at an output should not feed

back through internal cross-coupling to an input, since noise may be present on the output lines.

T Series Flip-Flop Economy Features

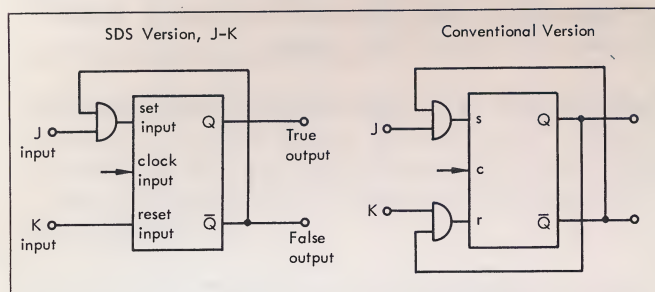
One basic T Series flip-flop achieves all this, and more. Its outputs can be tied directly to other flip-flop or amplifier outputs to form an AND function without additional gates. This proprietary flip-flop is produced in quantity as a monolithic integrated circuit for low unit cost.

The feature that makes it possible to use one flip-flop with a minimum of external wiring in four modes of operation (R-S, J-K, T, and D) is called "set-overrides-reset." A study of system logic design has revealed that, in the majority of cases, implementation is simpler if the set input

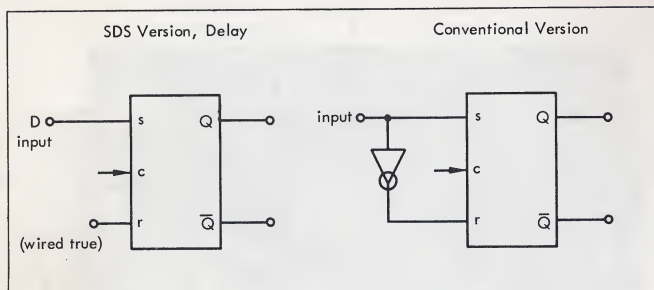
always overrides the reset input when both are true simultaneously, (see truth table below).

Period n		n + 1
set input	reset input	true output
0	0	Same as n
0	1	0
1	0	1
1	1	1

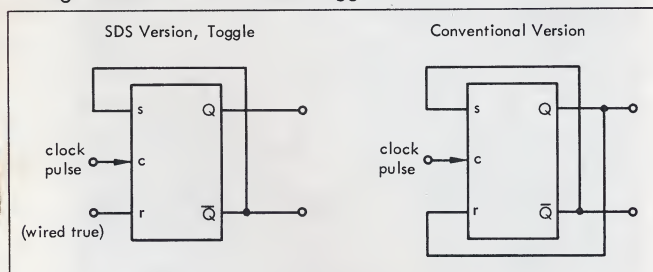
Using this basic flip-flop, the reset output can be wired to an AND gate at the set input to create a J-K flip-flop. A conventional flip-flop requires a second wire to achieve the same result. It connects the set output to an AND gate at the reset input. The SDS model avoids this second wire because set always overrides reset.



The same feature saves an inverter and reduces wiring in the Delay mode of operation. When the reset input is prewired "true," the set input operates the circuit as a delay flip-flop - that is, the set output state follows the set input state, delayed by one clock pulse period.



This feature also saves wiring in the Toggle mode. In this mode the clock input operates the circuit, causing it to change state at each clock trigger.



The flip-flop may also be used as a straight clocked set-reset (R-S) flip-flop with the s and r inputs activated directly, or asynchronously with d-c inputs, mark (m) and erase (e), which override the s and r inputs. Note that in clocked R-S operation there is no ambiguity because set overrides reset.

T Series Flip-Flop Performance Features

The SDS flip-flop has the same fan-out as an amplifier. Each output can drive 14 unit loads.

Internal delay of the basic flip-flop is 40 nanoseconds typical, 60 nanoseconds worst case. Since the minimum clock on-time is about 30 nanoseconds a simple toggle circuit such as used in a counter may be operated at a clock rate of 10 Mc (100 nanoseconds).

Two features that prevent erroneous switching are a short sampling period and true trailing edge clock triggering. Input signal conditions do not affect flip-flop operation, even when the clock input is true, until a very short time prior to the clock's falling edge. The SDS circuit is not the conventional double rank type in which the first rank is set on the 0-to-1 clock input transition, then shifted to the second rank on the 1-to-0 transition. The SDS technique provides timing security without undue restrictions on clock pulse-shape, and also allows maximum input signal settling time between clocks.

Both flip-flop outputs are buffered within the integrated circuit to completely isolate output signals from inputs.

GROUP 5. POWER

D-c power to logic modules must have low drift. It must be free from transients, which could cause false triggering. Transients normally enter the system via the a-c power line, particularly when high starting current devices such as motors are on the same line. A module power supply should also be designed to protect the delicate semiconductors from overvoltage or short circuits. Finally, the supply should be capable of rack mounting and operate with various popular line frequencies and voltages.

T Series Power Supplies

The PT10 (35-55 modules) and PT12 (200 module supply) provide 5% output regulation, with inputs of either 110 or 230 volts at frequencies from 50 to 400 cycles. Both provide overvoltage and short circuit protection. The PT10 plugs into a module mounting case, requiring only 15 module spaces. The PT12 uses the 19 inch rack width.

Power busses to modules are supplied on the back panel board, on the same plane as the ground plane, to minimize high frequency pickup by power lines.

Additional transient filtering is provided by individual decoupling circuits on each module.

GROUP 6. MECHANICAL

Mounting hardware should be economical, rugged, easy to assemble and disassemble, and compatible with industry standard hardware. It should be available in several options for convenience. Design must take into account electrical properties such as shielding and ground currents as well as heat dissipation.

T Series mounting hardware is based on a standard 19-inch rack width. One type of welded steel, ventilated 32-module mounting case is available with 2-position front or back bracket mounts, and right or left vertical hinges. A second 90-module type is built as a pull-out drawer. Blowers are available. The logic ground system is independent of the rack and case ground to avoid ground loops.

OTHER COST FACTORS

Equipment failure can be costly when it interrupts operation of another system. SDS modules have a proven reliability record. Natural logic results in fewer logic components per system. Integrated circuits reduce the number of

wire connection points as much as 20 to 1. All modules are worst case designed and 100% tested. Parts standardization and fewer components per system means smaller, less expensive stocks of replacement parts. And, reliable fully documented Module Testers save circuit test time.

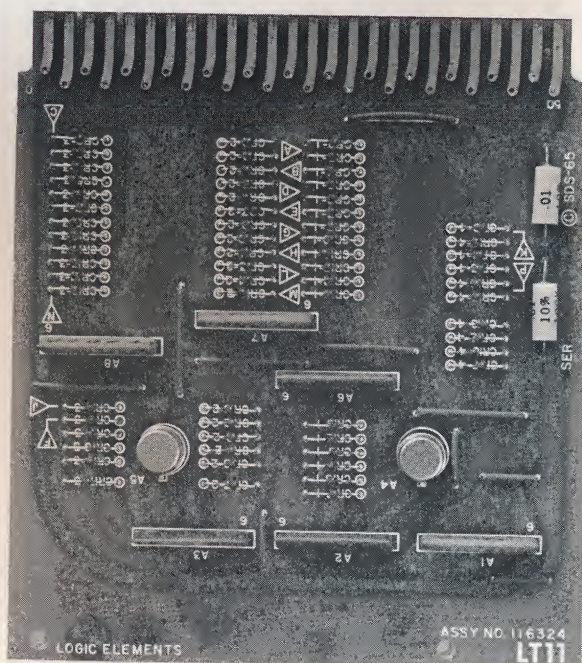
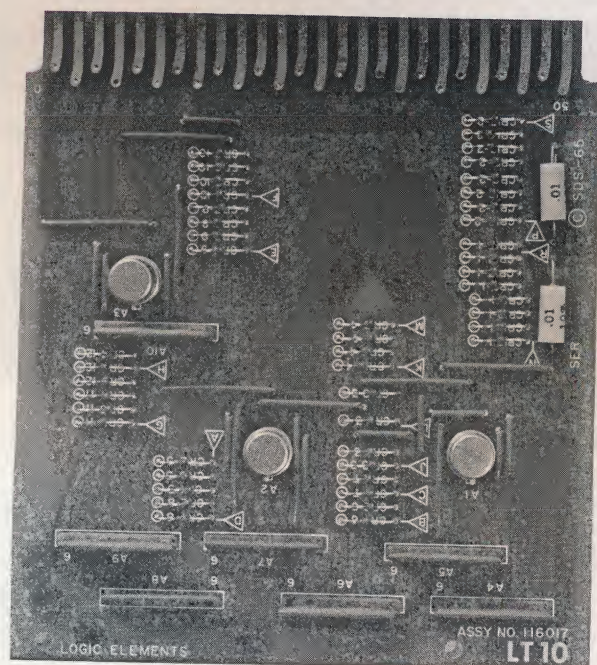
Time consuming special circuit design is avoided since T Series offers the circuit types that SDS engineers have found they needed to build many types of systems.

SUMMARY

T Series modules are designed for low cost, error-free high or low speed digital systems that may be assembled quickly, to operate reliably over long periods.

A number of important features such as natural logic, high current drive, integral ground plane, and set-override-reset flip-flop, are unique to the SDS product line. They are responsible for the economy and performance benefits that derive from use of SDS T Series.

If you wish to build this kind of system, T Series is for you.



II. DESCRIPTIONS OF MODULES AND ACCESSORIES

SUMMARY OF MODULE TYPES

Modules are classified as logic element-modules, flip-flop and register modules, or special circuit modules. The logic element modules contain AND, OR, NAND, and NOR gates with outputs logically amplified or amplified and inverted. The flip-flop modules are used for storage, counting, and shifting. These two broad classes of modules usually form the bulk of a system. Most special circuits are used to communicate with other equipments or display devices. Special circuit modules include cable drivers, receivers, and cable plug modules; interface drivers and receivers to communicate with logic at levels other than 0v and +4v; Schmitt Trigger level detectors for accepting input of arbitrary waveshape; one-shots for precise control of delays; and lamp drivers, relay drivers, and D/A converters for driving display, recording, and mechanical control devices. Also included among special circuits are the clock oscillators, which furnish the system time reference.

LOGIC ELEMENT MODULES

These modules carry the prefix B, I, or L. Some F prefix modules, the buffered latches, operate as logic element modules when the latch control inputs are grounded. Table 1 below, lists the modules and shows the distribution of logic functions.

Gates are also available on most other modules. In many cases no separate logic modules are needed because all necessary gating is performed right on the flip-flop or special circuit module.

TABLE 1. LOGIC ELEMENT OUTPUTS PER MODULE

Model No.	OUTPUT NOT INVERTED			OUTPUT INVERTED		
	With AND Inputs	With OR Inputs	With AND/OR Inputs	With Single Input	With AND Inputs (NAND)	With AND/OR Inputs (AND/NOR)
BT10			8			
BT11	12					
BT12	16*					
BT13	18**					
BT18	10					
FT26		8				
FT27		12				
IT10						8
IT11					12	
IT13					18**	
IT18					10	
LT10	4	2	2	3	1	
LT11			4†			4†

* Arranged as 2 separate binary-to-unitary decoding matrices

** 16 outputs in matrix form, 2 independent

† Same inputs, both Q and $\bar{Q}$ outputs

The AND/OR structures may be very simply converted to pure ANDs or ORs by wiring inputs True (leaving open) or False (grounding). Thus the BT10, IT10, LT10, and LT11 modules can also furnish ORs or NORs.

FLIP-FLOPS AND REGISTERS

T Series includes a number of dense and powerful high speed, fully gated flip-flop modules. In addition three latch modules are provided for low cost slower speed (2 Mc) storage.

TABLE 2. STORAGE ELEMENTS PER MODULE

Model No.	Description	Speed	No. of F.F. or Latches
FT10	Basic flip-flops with gated set and gated clock inputs	High	6
FT11	Flip-flops with gating for all counter modes	High	4
FT12	Basic flip-flops with some gated set inputs	High	8
FT19	Multipurpose registers/counters	High	8
FT20	Two 8-bit latch storage registers, with fast/slow. strobe option	Low	16
FT26	Buffered latches with 4-bit OR inputs	Low	8
FT27	Buffered latches with 2-bit OR inputs	Low	12

SPECIAL CIRCUITS

Two types of high density cable drivers and receiver modules are offered. AT10, AT11, and AT12 are intended for equipment using T Series modules at both ends of the cable. AT14 and AT15 use 0v/+8v logic levels and are designed to interface through cables with other lines of modules, such as the SDS discrete-component C, H, and L Series.

Two types of interface modules are offered. NT10 and NT11 will drive high level positive True logic (0v/+8v). Any T Series gate can receive high level logic up to +10v, thus no special interface receiver is required as companion for NT10/NT11. NT17 and NT18 interface with negative True logic systems having logic levels down to -12v.

The adjustable AT22 Schmitt Trigger circuit converts any input waveshape to discrete logic level changes of 0v and +4v. It is also useful as a dc level detector.

The OT17 one-shot provides outputs of adjustable pulse-width from 100 nsec to 100 μ sec.

QT14 Lamp Drivers and RT14 Relay Drivers handle up to 200 ma at 28 volts. DT12 and DT13 modules drive analog devices having up to ± 20 volt input requirement, in a

variety of operating modes.

CT16 and CT10 crystal (or LC) controlled clock oscillators provide clock signals in two ranges: 1.8Kc to 2 Mc, and 1 Mc to 10 Mc, respectively.

SPECIFICATIONS

Maximum operating frequency, circuit delays, fan-out, input loads, logic levels, and noise rejection are as described in General Specifications, p. 1, unless otherwise noted.

Module Current Requirements

The maximum current and maximum dissipation listed in each specification is for the case where all circuits are in the state which draws maximum current. The inverter and buffer circuits use maximum current when the output is binary 0.

The average current specification given is the current used when the amplifier is on half the time and off half the time. In a system of any complexity the average current instead of the maximum current should be used to determine total power requirements. This gives a more accurate indication of the actual current required.

Only one current specification is given for IC flip-flops because one half always conducts. Current requirements are therefore independent of output state.

Module Dissipation Ratings

The dissipation figure shown for a module is a worst-case calculation derived from the voltage-current product plus an allowance for IC or transistor dissipation due to load current supplied to other modules. This figure may be used to calculate maximum cooling requirements, but normally will not represent the power required by the module. If average current figures are used, dissipation will also be substantially lower than the dissipation values given.

SUMMARY OF LOADING AND WIRING RULES

LOADING RULES

1. Any 0v/+4v logic output may drive any 0v/+4v logic input.
2. Unless otherwise noted, every gate on a logic line places 1 unit load (3.8 ma) on the driver. Add all gates on a line for total load.
3. Each logic line terminator (220 ohms, on XT10) absorbs 5 unit loads. Maximum is 2 per line, 1 per branch.
4. Every T Series buffer, inverter, or flip-flop output

drives 14 unit loads. Fan-outs of other circuits are as noted in specifications.

5. Buffer, inverter, and flip-flop outputs may be paralleled to form logic functions (see p. 39). Each one paralleled to the first decreases fan-out by 2 loads.

WIRING RULES

General

1. Use No. 28 AWG copper/polyethylene wire, point-to-point. Push close to ground plane.
2. Lay out connections for shortest total wire length. Two branches per line is maximum. Two connections per pin is maximum.
3. Ground unused flip-flop set inputs (wire False) to avoid set-1 permanently overriding reset. Ground unused flip-flop dc inputs. Ground unused OR inputs. Leave open (True) unused AND inputs.
4. Power pins: +4v, pin 49; +8v, pin 51; -8v, pin 50. Ground pins are: 0, 16, 32, 48. The +4v, +8v, and ground wiring is built into back panel plane.

Simplified Rules For Safe Operation Below 2 Mc

Because of relatively long settling time (>500 nsec) T Series logic wiring for use with clock rate under 2 Mc is simple. Observe these rules:

1. Maximum wire length is 60 inches per branch (max. 2 branches per line).
2. Three stages of series buffers/inverters between flip-flops is maximum unless delays are calculated to be under 500 nsec total.
3. With 3 stages use terminator on at least 1 line if total length of any line reaches 60 inches. With 1 or 2 stages no terminators are required.

Operation Above 2 Mc Clock Rate

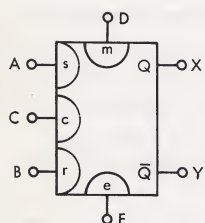
As clock rate is increased less delay can be tolerated in the wiring since active circuit delays are fixed. Line terminators decrease delay on the 0 to 1 transition by decreasing line capacitance charge time. At clock frequencies over 2 Mc wiring rules are more stringent than those given above, and delays may have to be calculated. Refer to Application Bulletin 64-51-04B for a technical discussion of delay problems and additional data on wiring delays.

In general lines under 18 inches need not be terminated but lines over 60 inches must be terminated. Between these boundaries termination is optional and depends on both propagation speeds desired and the magnitude and timing of reflections.

LOGIC SYMBOLS

GATES

AND Gate		$Q = A \cdot B \cdot C$
OR Gate		$Q = A + B + C$
AND/OR Gate		$Q = A \cdot B + C \cdot D$



Signal Relationships:

$$X = Y = D + AC$$

(C is falling edge of clock pulse)

$$Y = \bar{X} = E + B\bar{C}$$

Terminal Designations:

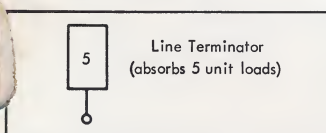
- m = "mark" input (unclocked set input)
- e = "erase" input (unclocked reset input)
- s = set input (must be clocked)
- r = reset input (must be clocked)
- c = clock input (falling edge of clock is used)
- Q = set output $\bar{Q}$ = reset output

TRUTH TABLE

Period n	n+1	
s	r	Q
0	0	Q^n
0	1	0
*1	0	1
*1	1	1

*Note the unique characteristic of the SDS flip-flop: the set input, when True, always causes the output to go True, regardless of the state of the reset input. Mark and erase inputs, however, always override set and reset inputs. When both mark and erase are true simultaneously the output is indeterminate. Inputs must be wired False (grounded) when not used. Reset input is wired True (left open) in set-True-overrides-reset-True applications.

TERMINATORS



AMPLIFIERS

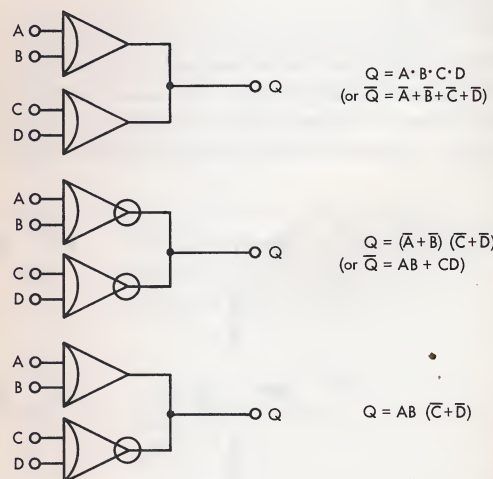
Buffer Amplifier		$Q = A$
Inverter Amplifier		$Q = \bar{A}$

COMBINATION ELEMENTS

Buffered AND Gate (BAND)		$Q = A \cdot B \cdot C$
Buffered OR Gate		$Q = A + B + C$
NAND Gate		$Q = \overline{A \cdot B \cdot C}$ (or $\bar{Q} = A \cdot B \cdot C$)
NOR Gate		$Q = \overline{A + B + C}$ (or $\bar{Q} = A + B + C$)

LOGIC FUNCTIONS FORMED AT OUTPUTS

A unique SDS feature is the AND or OR function created when two or more amplifier or flip-flop outputs are tied directly together. The rule is that any element having a false output will cause all outputs connected together to be false.



SPECIAL AMPLIFIERS

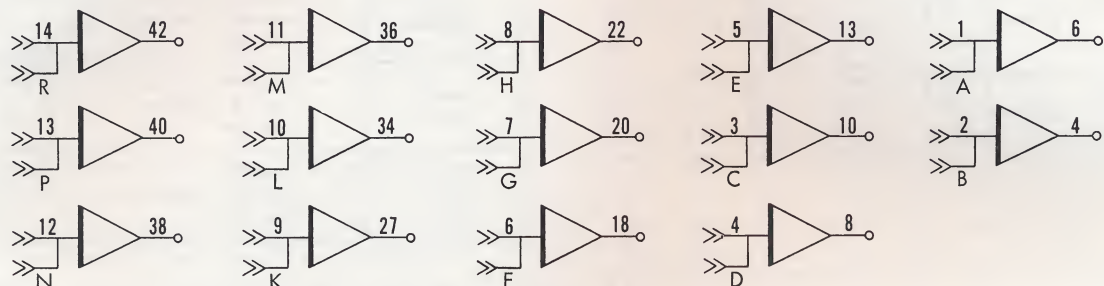
	Interface Cable Driver (on AT14 Module)		Interface Cable Receiver (on AT15 Module)
	Clock Driver		Interface Buffer
	Emitter Follower (on DT12/13 Modules)		

AT10

Model AT10, AT11, and AT12 modules, together with ET cable components, constitute a high-speed logic signal interconnection system for distances up to 200 feet. Logic levels of 0v/+2v are transmitted over 33 ohm cable. Cables are clamped to the front edge of each module.

The AT10 module contains 14 identical cable receiver circuits which switch when input exceeds the +0.54v switching value. Output is not inverted. Up to 25 receivers can be connected to the output of 1 cable driver, because input capacitance is very low.

Max. Operating Freq.	10 Mc
Circuit Delay	20 nsec typ., 40 nsec worst case
Input Logic Levels	0v (Logic 0), +2v (Logic 1)
Switching Threshold	+0.54v $\pm$ 0.1v
Input Range	-1.5v to +4.4v
Input Current	50 μ a per receiver
Input Capacitance	8 pf max.
Output Logic Levels	0v (Logic 0), +4v (Logic 1)
Output Drive	14 Unit Loads (53.2 ma)
Power Requirements	+4v, 178 ma av., 230 ma max. +8v, 100 ma; -8v, 100 ma
Dissipation	2.5 watts max.



LOGIC DIAGRAM, AT10

AT11

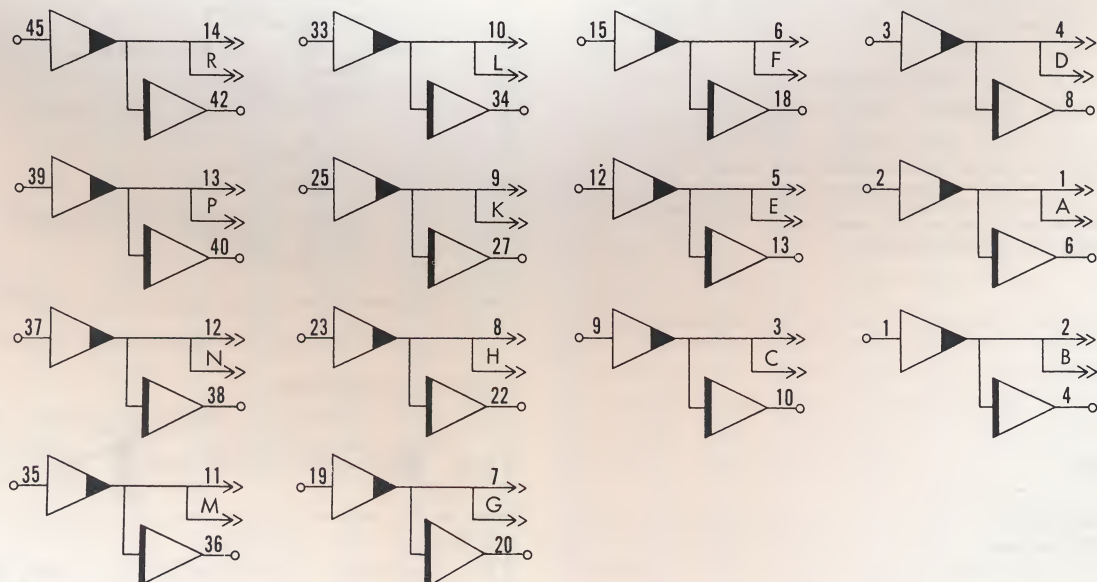
CABLE RECEIVERS/DRIVERS, MODEL AT11

AT11 contains 14 identical pairs of driver-receivers. Driver outputs are on the same terminals as receiver inputs to reduce space and connectors. Receivers normally use input from drivers at other cable locations, not from the same module. Circuits are identical to AT10 and AT12.

Power Requirements: +4v, 878 ma av., 1.8 amp max.
+8v, 485 ma; -8v, 100 ma

Dissipation: 4.5 watts max.

Other specifications: see AT10 or AT12



LOGIC DIAGRAM, AT11

CABLE DRIVERS, MODEL AT12

AT12

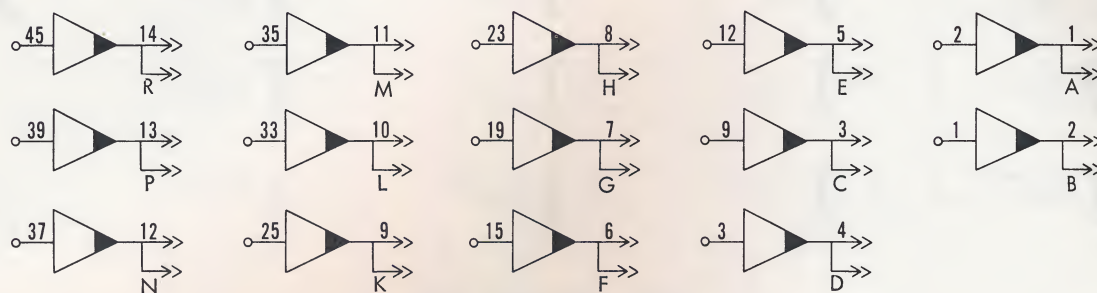
Model AT12 contains 14 identical cable driver circuits which accept standard T Series 0v/+4v logic level input and convert to 0v/+2v logic level output. The AT12 is designed to drive AT10 or AT11 receiver circuits, and has front-edge contacts for ET11 connectors.

Driving capability depends on cable attenuation. Maximum length is 200 feet of 33 ohm cable. Any number of cable drivers can be placed on one cable but only one driver can be raised True at one time since outputs add.

Input wiring restrictions: back panel wiring cannot exceed 18 inches, and no terminator may be placed on input line.

Max. Operating Freq.	10 Mc
Circuit Delay	5 nsec typ., 10 nsec worst case
Input Logic Levels	0v (Logic 0), +4v (Logic 1)
Input Current	9 Unit Loads (34 ma)
Output Logic Levels	0v (Logic 0), +2v (Logic 1)
Output Loading	16.5 ohms to ground; use two 33 ohm cables or 1 cable and 1 dummy load (ET13)
Power Requirements	+4v, 700 ma av., 1.4 amp max +8v, 400 ma
Dissipation	4.0 watts max.

Refer to Accessories section for cable and connectors.



LOGIC DIAGRAM, AT12

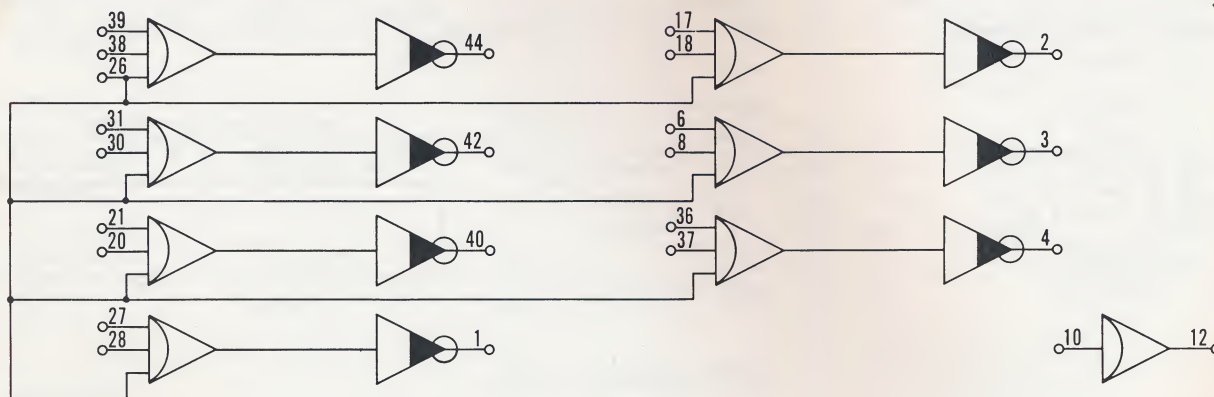
8-VOLT INTERFACE CABLE DRIVERS, MODEL AT14

AT14

The AT14 module has 7 cable drivers for driving 6 gates each, with 0 and +8v levels, such as are found on other SDS series modules (C, H, L, etc.). It also contains 1 buffer amplifier. Each cable driver circuit is driven by a T Series 3-input buffered AND with 0v and +4v logic levels; one of the three inputs is common to all gates on the card, for use as a common control line.

The drivers are designed to drive 33 ohm cable. Rise and fall times are about 1 μ sec to reach 50% of logic level. If cable length is less than 60 feet the cable may be connected directly to an SDS Model ZX13 cable plug module.

Power Requirements:	+4v: 58 ma av., 77 ma max. +8v: 125 ma, -8v: 63 ma (pin 50); +25v: 22 ma (pin 45)
Dissipation:	2.4 watts max.



LOGIC DIAGRAM, AT14

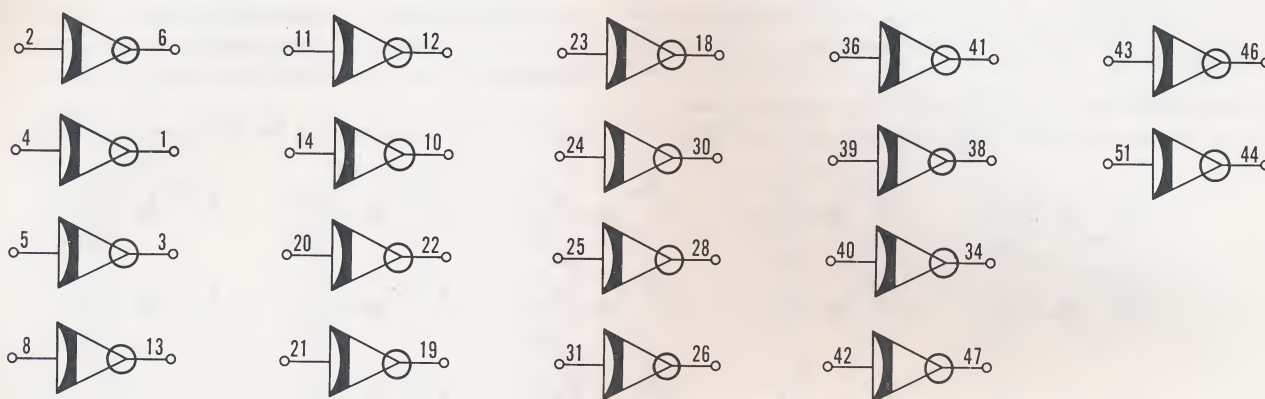
AT15

Model AT15 module has 18 cable receiver circuits which will accept logic signals at 0v and +8v levels from a 33 ohm cable input. These circuits may be driven by the Model AT14 cable driver or by 0v and +8v logic signals from SDS B, C, H, K, L, or X Series modules. The output of each receiver is a standard T Series inverter output with 0v and +4v logic levels, capable of driving 14 unit loads.

8-VOLT INTERFACE CABLE RECEIVERS, MODEL AT15

Power Requirements: +4v: 95 ma av., 126 ma max.
-8v: 9 ma (pin 50);
+25v: 51 ma (pin 45)*
Dissipation: 1.85 watts max.

*Use PX10 Power Supply



LOGIC DIAGRAM, AT15

AT22

SCHMITT TRIGGERS, MODEL AT22

Model AT22 contains two dc-to-10 Mc Schmitt Trigger circuits. Three input ranges are provided. Each Q output rises to +4v when input exceeds the adjustable trigger level and returns to 0v when input drops below the adjustable hysteresis level, which is always more negative than the trigger level.

The Schmitt Trigger is essential for squaring sine wave or other non-squarewave input. It is also used as a dc level sensor or a pulse amplifier. A regulator on the module keeps thresholds stable. Outputs are fully buffered.

Circuit Delay: 25 nsec typical
Input load to common: $\pm 5v$ range, 1K ohms
 $\pm 15v$ range, 3K ohms
 $\pm 50v$ range, 10K ohms
Resolution: $\pm 5v$ range, 0.001v
 $\pm 15v$ range, 0.003v
 $\pm 50v$ range, 0.010v
Power Requirements: +4v, 10 ma
+8v, 35 ma
-8v, 50 ma
Dissipation: 0.750 watts max.

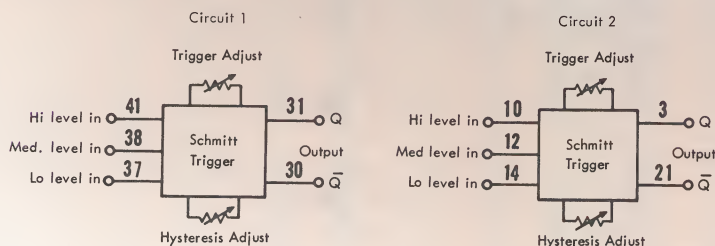


Table 1. Trigger and Hysteresis Ranges

Trigger (True threshold)	Hysteresis
$\pm 5v$	.2v to 1.3v
$\pm 15v$	.6v to 4.0v
$\pm 50v$	1.5v to 15.0v

LOGIC DIAGRAM, AT22

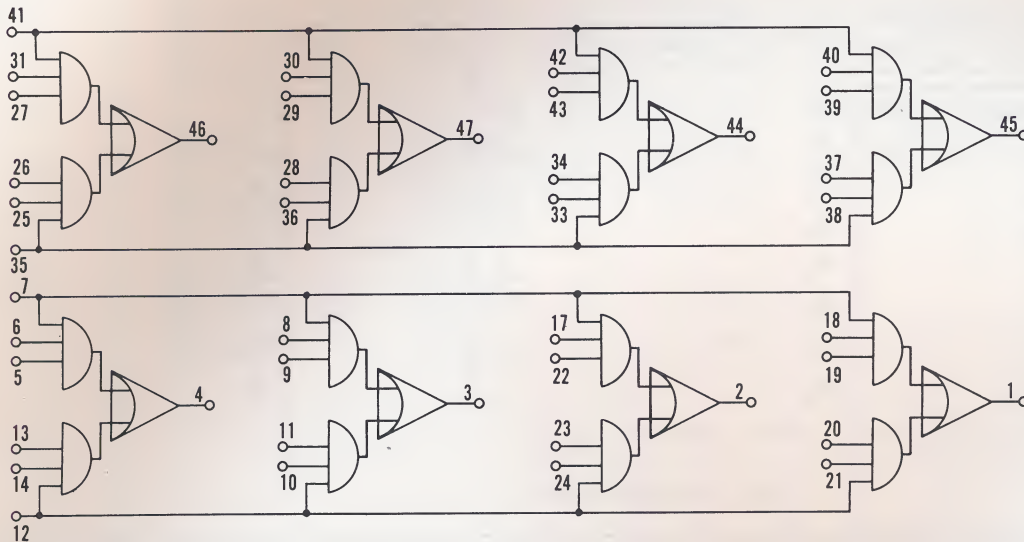
BUFFERED AND/OR GATES, MODEL BT10; INVERTED AND/OR GATES, MODEL IT10

BT10/IT10

Eight non-inverting (BT10) or inverting (IT10) AND/OR gate structures are on these modules. Each circuit consists of two, 3-input AND gates, the outputs of which are ORed and amplified. One input on each AND gate is shared with 3 other circuits. The circuits are designed to implement expressions of the type $A \cdot B \cdot C + D \cdot E \cdot F$. By connecting BT10 circuit outputs together an AND function can be generated,

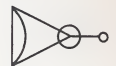
of the type $(A \cdot B \cdot C + D \cdot E \cdot F) (G \cdot H \cdot I + J \cdot K \cdot L)$.

Power Requirements: +4v: 95 ma av. (BT10),
63 ma av. (IT10), 126 ma max.
+8v: 54.4 ma
Dissipation: 0.94 watts max.



LOGIC DIAGRAM, BT10

Note: Diagram of IT version is identical except for amplifier symbols:



(IT uses Inverter Symbol)

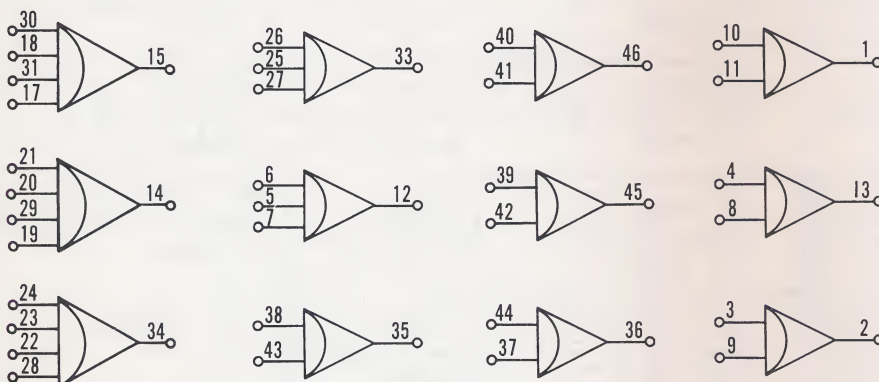
BUFFERED AND GATES, MODEL BT11; NAND GATES, MODEL IT11

BT11/IT11

The BT11 has an assortment of Buffered AND gates for general purpose use. There are two 3-input circuits; three 4-input circuits; and seven 2-input circuits. The AND functions can be expanded by connecting buffer outputs together.

All model IT11 amplifiers are inverters.

Power Requirements: +4v: 142 ma av. (BT11),
95 ma av. (IT11), 189 ma max.
+8v: 40.8 ma
Dissipation: 1.08 watts max.



LOGIC DIAGRAM, BT11

Note: Diagram of IT version is identical except for amplifier symbols:



(IT uses Inverter Symbol)

BT12

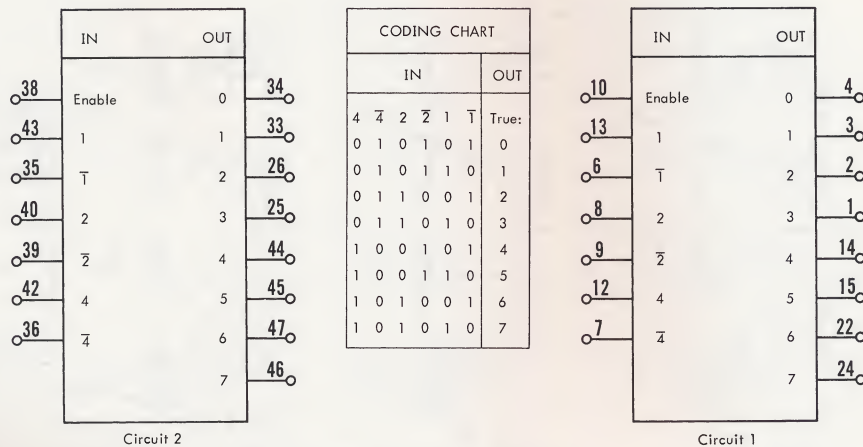
BINARY DECODERS, MODEL BT12

BT12 has 2 independent binary decoders. Each accepts 3-bit inputs and produces an output on one of 8 pins. In addition, Enable input prevents any outputs from being True when it is False. Enable is used when decoding numbers larger than 3 bits. Using Enable as the fourth input, 2 circuits can decode a 4-bit input so that only 1 out of 16 outputs is True at one time. Each output drives 14 unit

loads. Enable input requires 8 unit loads, all others 4 unit loads.

Power Requirements: +4v, 189 ma av., 252 ma max.
+8v, 54.4 ma

Dissipation: 1.4 watts max.



LOGIC DIAGRAM, BT12

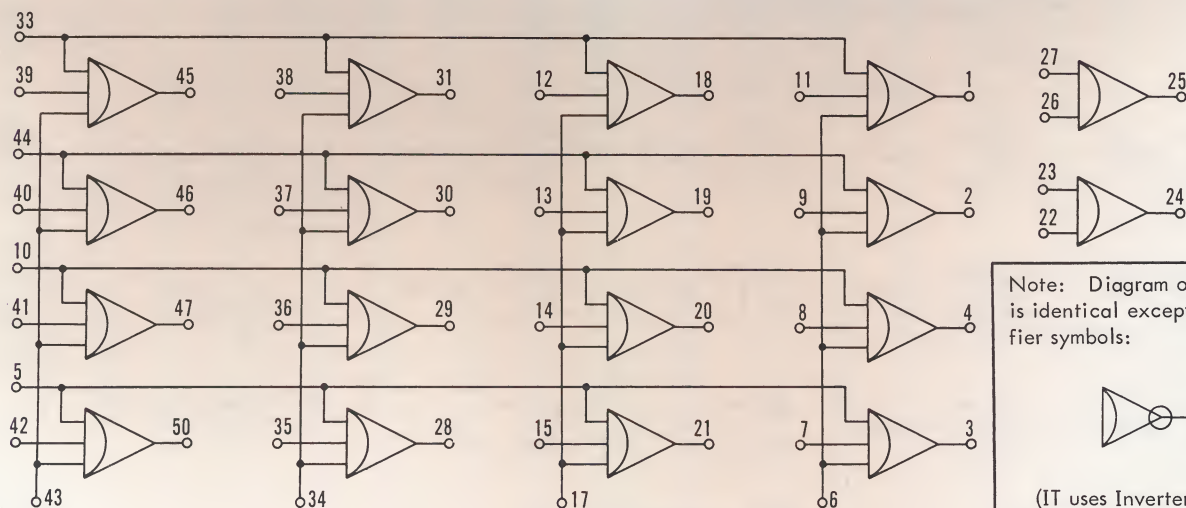
BT13/IT13

BUFFERED MATRIX, MODEL BT13; INVERTER MATRIX, MODEL IT13

BT13 has a 4 x 4 matrix which can (1) select one of up to 4 groups of 4 bits each, or (2) generate up to 16 discrete outputs from a 4 x 4 matrix input, or (3) provide 18 general purpose amplifiers (BT13) or inverters (IT13).

Power Requirements: +4v, 225 ma av., (BT13),
151 ma av., (IT13), 301 ma max.
+8v, 61.2 ma

Dissipation: 1.69 watts max.



LOGIC DIAGRAM, BT13

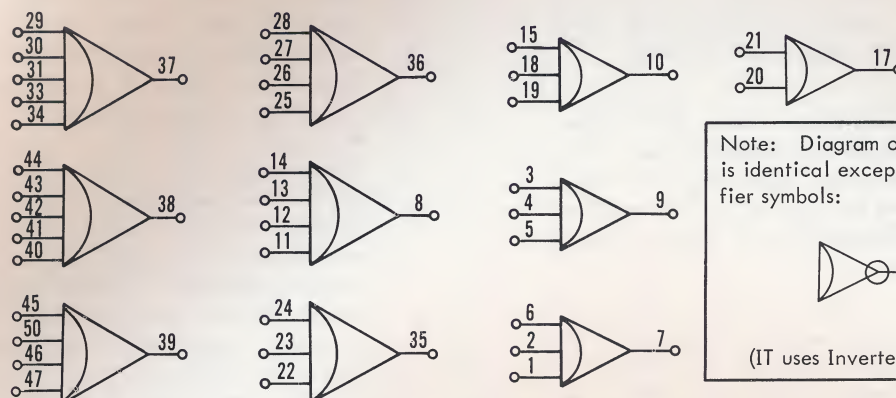
BUFFERED AND GATES, MODEL BT18; NAND GATES, MODEL IT18

BT18/IT18

These modules contain 10 AND (BT18) or 10 NAND (IT18) circuits intended for general purpose use. Each circuit can drive 14 loads. Outputs may be paralleled with other circuits; however, each paralleled output decreases the output drive capability by 2 unit loads.

Power Requirements: +4v: 132 ma av., (BT18)
88 ma av., (IT18), 175 ma max.
+8v: 34 ma

Dissipation: 0.97 watts max.



LOGIC DIAGRAM, BT18

HIGH FREQUENCY CLOCK OSCILLATOR, MODEL CT10

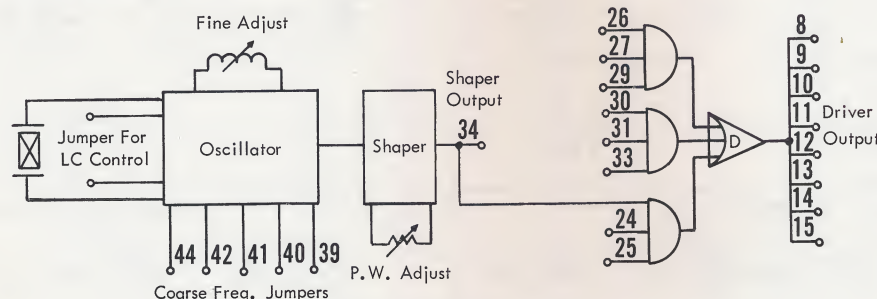
CT10

The CT10 has a 1 Mc to 10 Mc oscillator, a pulse shaper, and a gated clock amplifier (driver). Oscillator is controlled by adjustable LC or by optional crystal. When LC control is used external jumpers select range. When crystal control is desired, specify frequency. Pulse shaper control varies clock True duration. Pin 34 drives 2 unit loads plus a 220 ohm line terminator. Driver has a control gate which permits frequency division under external logic control. Gate inputs absorb 2 unit loads.

This module requires two card slots.

Clock bus can be logic wiring or 33 ohm cable. Terminators are required: 220 ohm (on XT10) for logic lines, or 75 ohm (on flip-flop cards) for cable. Lines should radiate from driver in equal lengths to avoid clock skew.

Frequency range: 1 Mc to 10 Mc
Stability, crystal operation: 2 p.p.m. per °C
Crystal freq. accuracy: ±0.05%
Driver fan-out: 60 unit loads
Shaper fan-out: 7 unit loads
Gate inputs: 2 unit loads ea.
Power requirements: +4v, 40 ma
+8v, 130 ma
-8v, 60 ma
(at 50% duty cycle)
Dissipation: 1.7 watts max.



LOGIC DIAGRAM, CT10

DT12/DT13

Each module has two D/A converters designed for low cost applications where high accuracy is not required. DT12 converters accept 4 bits; DT13 converters accept 6 bits. The DT12-1 and DT13-1 modules also include a reference regulator, and buffer amplifiers, as shown in the diagrams below. Converters can be cascaded to form 8-bit, 10-bit, and 12-bit units for high resolution. The DT12 modules can also be connected (with additional resistors) to accept BCD input and can be cascaded to accept 3 BCD digits and sign.

The converters operate with unipolar output. With additional resistors they can also provide bipolar output. The conversion table below, gives output value vs. input code. Note that in the bipolar mode the input codes for negative values must be in 2's complement form if binary, and in 10's complement form if BCD.

An external reference source of maximum +20v on +Eref (plus additional -20v on -Eref for bipolar output) can be used. If the +5v internal reference source is used, one buffer amplifier must be connected between regulator output and converter Eref input. The same amplifier can also supply 14 additional converters. A buffer can be used on Eout when Eref is +5v or less, or in bipolar operation with +5v and -5v reference voltages.

D/A CONVERTERS, DT12-1, DT12-2, AND DT13-1, DT13-2

Input-Output Specifications

- Converter (switches and precision resistor network)
 - Accuracy: $\pm 1.0\%$ relative to reference voltage
 - Switch offset: +50 millivolts typical
 - Output impedance: 5K ohms $\pm 1\%$
 - Inputs: standard T Series logic levels, 1 unit load
 - Output voltage: as given in conversion table
 - Conversion rate: 400 Kc max.
 - Settling time (to ± 150 mv of f.v.): 2.5 μ sec after input signal completes switching. Open output.
- Buffer amplifier (emitter follower)
 - Accuracy: $\pm 1.0\%$
 - Output range: -1.67v to +5v
 - Offset: ± 100 millivolts typical
 - Loading capability: ± 10 ma max.
 - Input impedance: 150K ohms min. at dc
 - Output impedance: 50 ohms typical
 - Settling time: 2 μ sec. max. to ± 50 mv of final value, 1 μ sec. max to ± 150 mv of final value
- +5v reference regulator

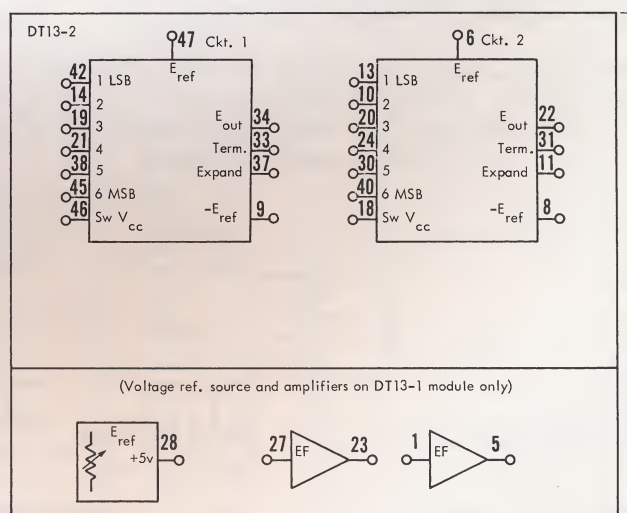
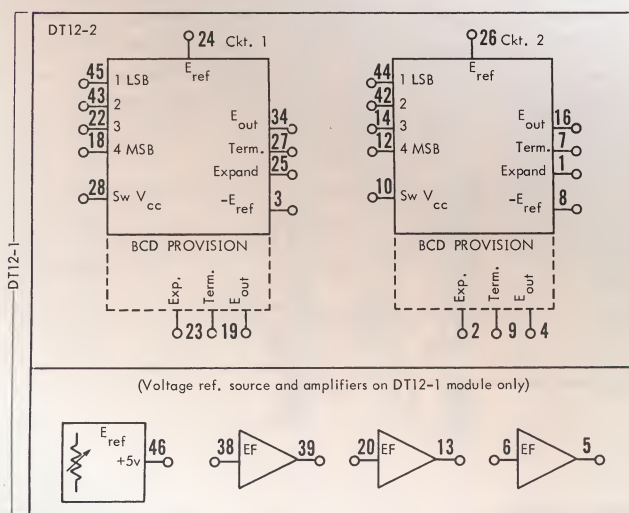
Output voltage adjustable to $\pm 0.1\%$; current: 0.2

Power Specifications (max.)

- Each bit (switch and resistor): +8v, 7.6 ma;
-8v, 1 ma (pin 50)
- Each amplifier: +8v, 50 ma; -8v, 50 ma (pin 50)
- +5v reference regulator: +8v, 35 ma

CONVERSION TABLE	INPUTS						Eout, BINARY Operation		Eout, BCD Operation	
	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	UNIPOLAR		UNIPOLAR	
	0	0	0	0	0	0	Full Scale	Eref (1-1/2 ⁿ)*	0.6 Eref (1-1/10 ^d)*	
	1	1	1	1	1	0	LSB	Eref/2 ⁿ	0.6 Eref/10 ^d	
	1	1	1	1	1	1	0	0 volts	0 volts	
	sign bit						BIPOLAR (MSB is sign bit)		BIPOLAR (MSB is sign bit)	
	0	0	0	0	0	0	+Full Scale	1/3 (+Eref)(1-1/2 ⁿ)	0.2 (+Eref) (1-1/10 ^d)	
	0	1	1	1	1	0	+LSB	1/3 (+Eref/2 ⁿ)	0.2 (+Eref/10 ^d)	
	0	1	1	1	1	1	0	0 volts	0 volts	
	1	0	0	0	0	0	-LSB	1/3 (-Eref/2 ⁿ)	0.2 (-Eref/10 ^d)	
	1	1	1	1	1	1	-Full Scale	1/3 (-Eref)	0.2 (-Eref)	

*n = number of magnitude bits
d = number of decimal digits



MEDIUM FREQUENCY CLOCK OSCILLATOR, MODEL CT16

CT16

The CT16 has a 1 Mc to 2 Mc oscillator with 50% duty cycle squarewave output, and a seven stage down-counter. Oscillator is controlled by LC or crystal. (For higher output drive capability add buffer modules). Clock can be bussed via logic wiring or via 33 ohm cable. Terminators must be used: 220 ohms with logic lines (on XT10) or 75 ohms with cable (on flip-flops). Lines should radiate from driver in equal lengths to avoid clock skew.

Frequency range:
Stability, crystal operation:
Crystal freq. accuracy:
Fan-out:

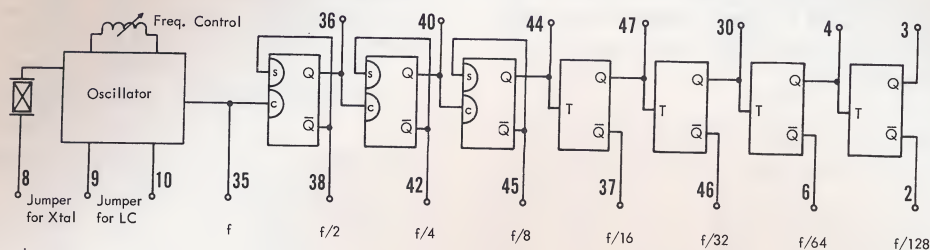
7.8 Kc to 2 Mc
2 p.p.m. per °C
±0.05%
Pins 35, 36, 38, 40, 42, 44,
45: 14 loads; all others, 10
loads

Power requirements:
(at 50% duty cycle)

+4v, 240 ma
+8v, 85 ma
-8v, 52 ma

Dissipation:

2.1 watts max.



LOGIC DIAGRAM, CT16

BASIC FLIP-FLOPS, MODEL FT10

FT10

FT10 contains 6 identical flip-flops designed for basic operations as shift registers and binary or BCD counters, either parallel loaded or preset by mark inputs. Terminator is for 33 ohm clock cable. Ground m and e if not used.

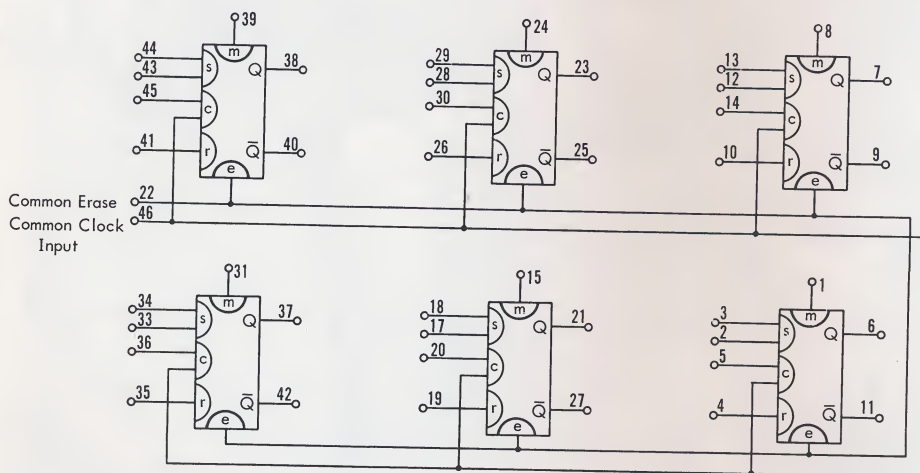
Maximum Operating Frequency 10 Mc
Mark and erase min. True time 40 nsec
s and r min. stable before clock falls 30 nsec

s and r min. stable after clock falls
Clock min. True duration
Clock min. False duration
Circuit Delay

5 nsec
30 nsec
60 nsec
40 nsec typ.,
60 nsec worst case
+4v, 268 ma
+8v, 102 ma
1.89 watts max.

Power Requirements

Dissipation



LOGIC DIAGRAM, FT10

FT11

4-BIT HIGH SPEED COUNTER, MODEL FT11

FT11 contains 4 flip-flops and gating designed for high speed, synchronous counting functions. The module can function as a binary or BCD up- or down-counter, or can be used as a combination counter/shift register. It can be preset at high speed. As with other SDS flip-flop modules, only one logic polarity is required for presetting since set-1 overrides reset. Reset input is permanently wired True, but is not shown in the logic diagram, below.

Presetting is accomplished through the 2-input gates marked LOAD Control and PRESET Data. Common Control and COUNT Pulse inputs must be False. Data is entered into the PRESET Data inputs, LOAD Control is made True, and LOAD Pulse is used as a clock. Note that the counter need not be cleared before presetting.

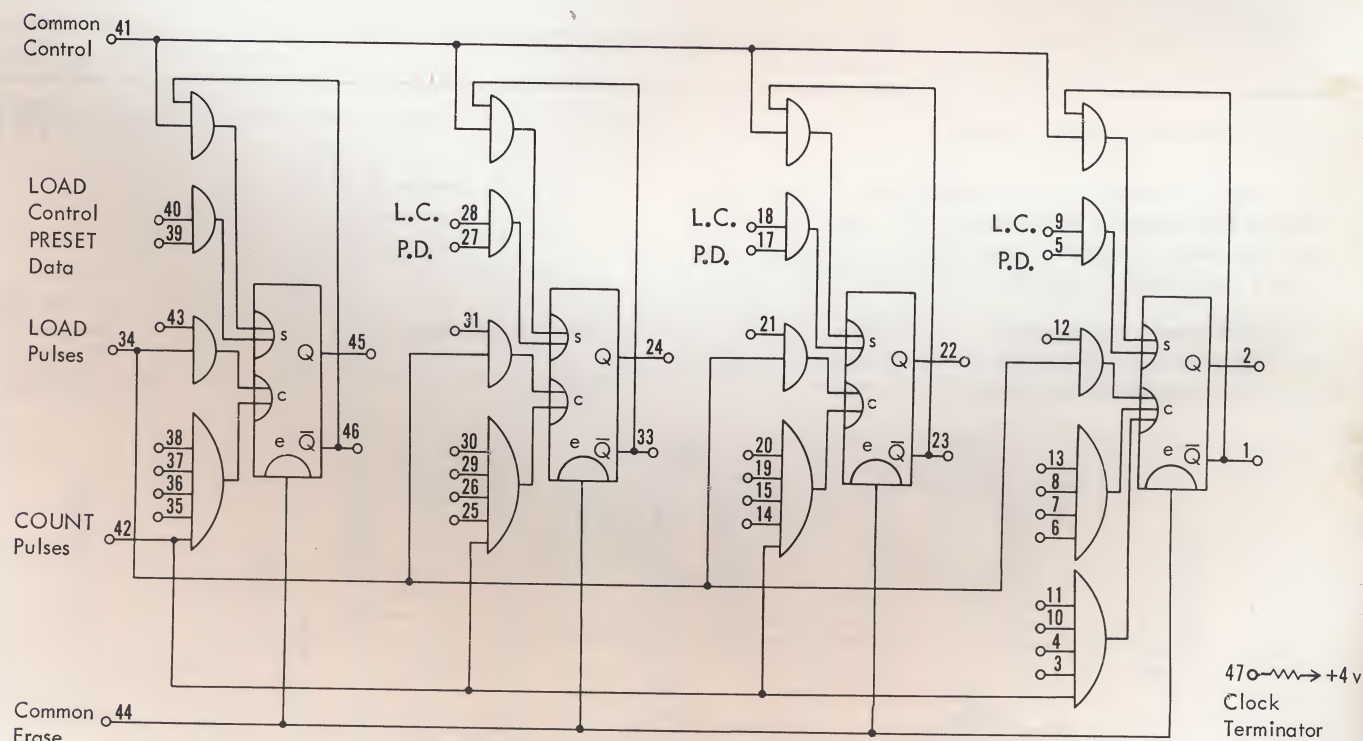
Counting is accomplished with Common Control True, LOAD Control False, LOAD Pulse False, and COUNT Pulse used

as clock. The 4-input gates are wired to properly condition the clock inputs for operation in the desired counting or shifting mode, whether binary, BCD, etc.

Common dc reset (without clock) is accomplished with the Common Erase input. This input must be False (ground) when not used.

Terminator is for use with optional 33 ohm clock cable.

Max. Operating Freq.	10 Mc
Timing and Delay	See FT10 specifications
Input Current	1 Unit Load per gate input
Fan-Out	14 Unit Loads, pins 45, 24, 22, 2; 13 Unit Loads, pins 46, 33, 23, 1
Power Requirements	+4v, 198 ma +8v, 81.6 ma
Dissipation	1.45 watts max.



LOGIC DIAGRAM, FT11

GATED FLIP-FLOPS, MODEL FT12

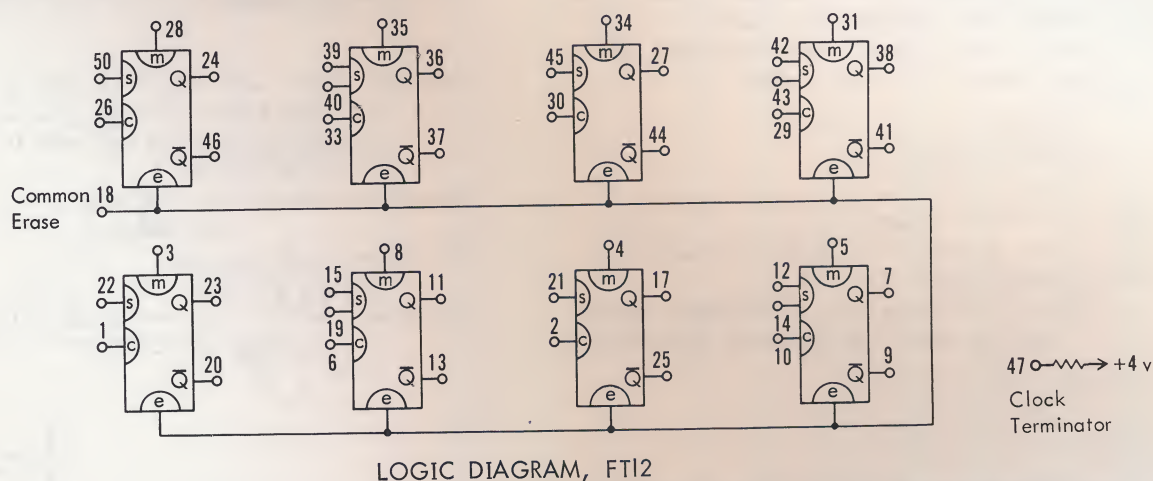
FT12, with 8 flip-flop circuits, is designed for applications requiring a large number of economical storage elements on one module. Enough basic gating is supplied for shift registers and binary or BCD counters. Synchronous or bi-directional versions are mechanized by adding gate modules. Reset input is wired True on all 8 circuits (not shown). Since set-1 overrides reset, set input controls reset state.

With external gating this circuit can perform all the func-

tions of two FT11 modules. In many applications it can also take the place of the FT10, at lower cost per flip-flop.

Ground mark and erase if not used.

Power Requirements: +4v, 338 ma; +8v, 108.8 ma
Dissipation: 2.22 watts max.



T SERIES Modules In SDS SIGMA 7 Computer



FT19

The FT19 contains two independent groups of four flip-flops each. With a few external jumper connections the module can function in the various modes listed below, under external logic control:

1. Storage and Control - data read in and out in parallel
2. Counter
 - a. Binary up counter-presetable
 - b. Binary down counter-presetable
 - c. Binary up-down counter-presetable (does not lose contents when changing direction)
 - d. Binary coded decimal counter-presetable (8 flip-flops represent 2 decimal digits)
3. Shift Register
 - a. Serial in, serial out
 - b. Serial in, parallel out
 - c. Parallel in, serial out
4. Shifting Up-Down Register
 - a. Load by parallel entry, shift in, or count up
 - b. Count up or down if desired
 - c. Read out by shifting serially, reading in parallel, or counting down (no loss during mode change)

4-BIT MULTIPURPOSE COUNTERS/REGISTERS, MODEL FT19

It is possible to form the combinations listed below:

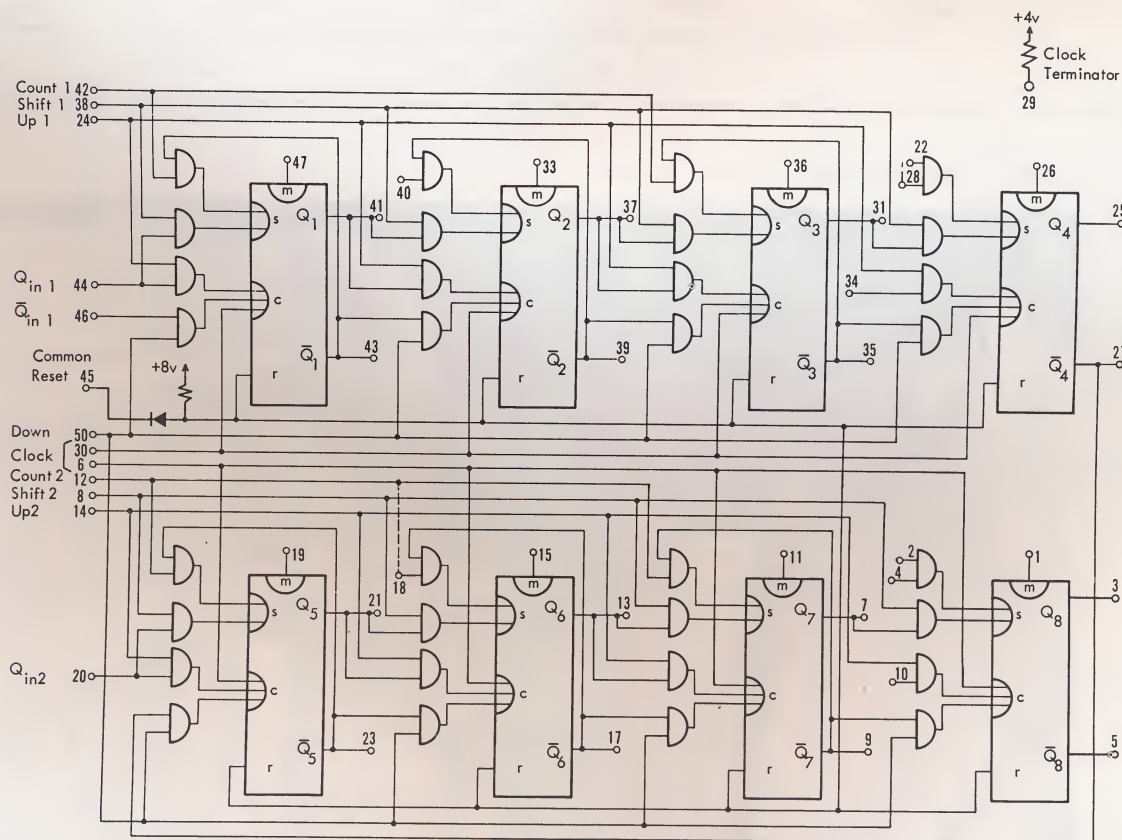
1. Two 4-bit counters (binary or BCD) or shift registers
2. One 8-bit counter (binary or BCD) or shift register
3. One 4-bit counter and one 4-bit shift register
4. One 8-bit up-down counter or one 4-bit up-down counter plus one 4-bit shift or storage register
5. One 8-bit shifting accumulator (or up-down counter) or one 4-bit shifting accumulator plus one 4-bit shift or storage register

Fan-Out: 14 Unit Loads (53.2 ma), pins 3, 5, 25
 13 Unit Loads (49.4 ma), pins 31, 7, 27
 12 Unit Loads (45.6 ma), pins 41, 43, 37, 39, 35,
 21, 23, 13, 17, 9

Power Requirements: +4v, 340 ma
 +8v, 165 ma

Dissipation: 2.68 watts max.

Reference: Bulletin No. 64-51-05B, FT19 Multipurpose Flip-Flop Applications



NOTE: 1. Mark inputs grounded when not used.
 2. Subscripts refer to ckt. number.
 Example: Up 2 is Up control line for ckt. 2

LOGIC DIAGRAM, FT19

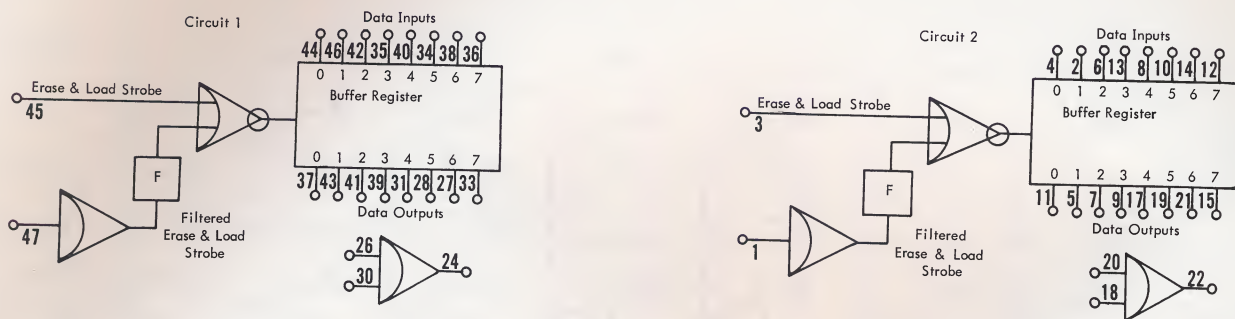
8-BIT BUFFERED LATCH REGISTERS, MODEL FT20

FT20

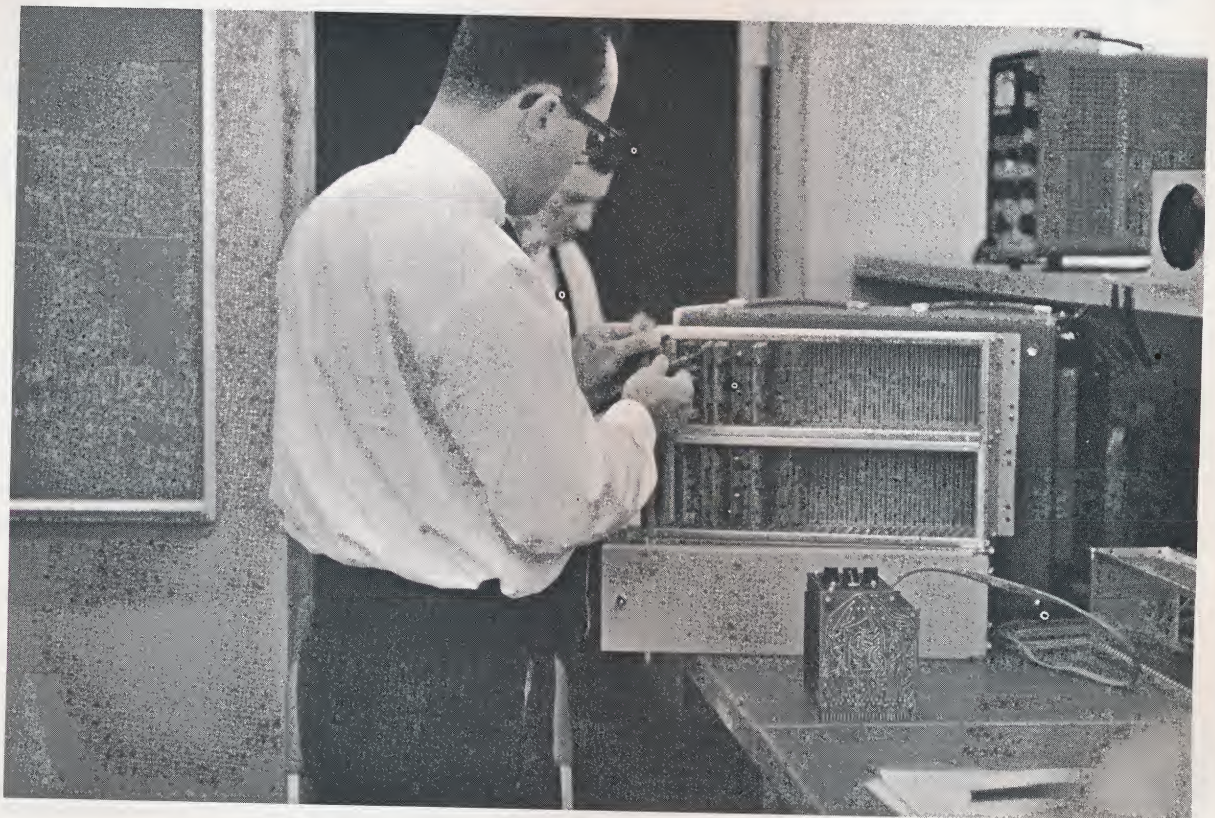
The FT20 contains 2 independent 8-bit buffered latch registers, useful for low-cost storage. Data is loaded and read in parallel. Only 1 strobe, minimum 30 nsec True, is needed to both erase and update contents. Outputs can be read after 50 nsec following strobe leading edge.

A filtered strobe input is provided for use in noisy environments. Filtered strobe must be True for 70 nsec minimum.

Max. Operating Freq: 10 Mc
 Output Drive: 13 Unit Loads per output
 Power Requirements: +4v, 255 ma av., 340 ma max.
 +8v, 80 ma max.
 Dissipation: 2.48 watts



LOGIC DIAGRAM, FT20



FT26

The FT26 module contains 8 circuits which can be used individually as OR gates or as latch circuits. The entire module can also be used for digital multiplexing.

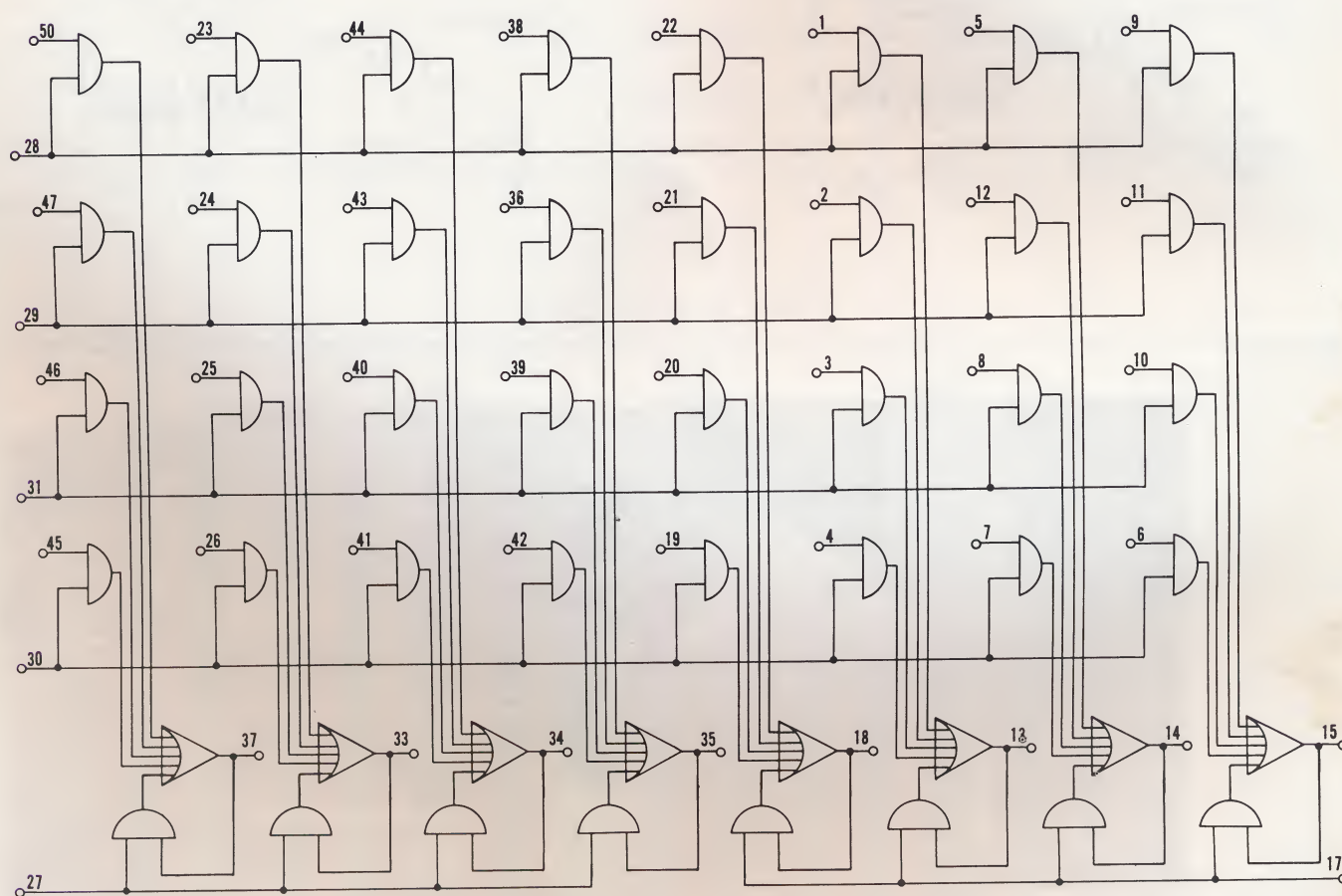
Each circuit can be used as a 4-input buffered OR by leaving pins 28, 29, 30, and 31, open (True) and grounding pins 17 and 27 (wiring False). Each can also be used as a latch circuit preceded with a 4-input OR, by leaving pins 28, 29, 30, and 31 open (True) while using pins 17 and 27 as latch control inputs. The module can be used as a 4 x 8 buffered

BUFFERED LATCH MATRIX, MODEL FT26

digital multiplexing matrix with optional latch storage by wiring pins 28, 29, 30, and 31 as multiplex controls and pins 17 and 27 as latch controls. Other applications may be devised.

Fan-Out, each buffer output: 13 Unit Loads (49.4 ma)
Power Requirements: +4v, 95 ma av., 127 ma max.
+8v, 136 ma

Dissipation: 1.59 watts max.



LOGIC DIAGRAM, FT26

BUFFERED LATCHES, MODEL FT27

FT27

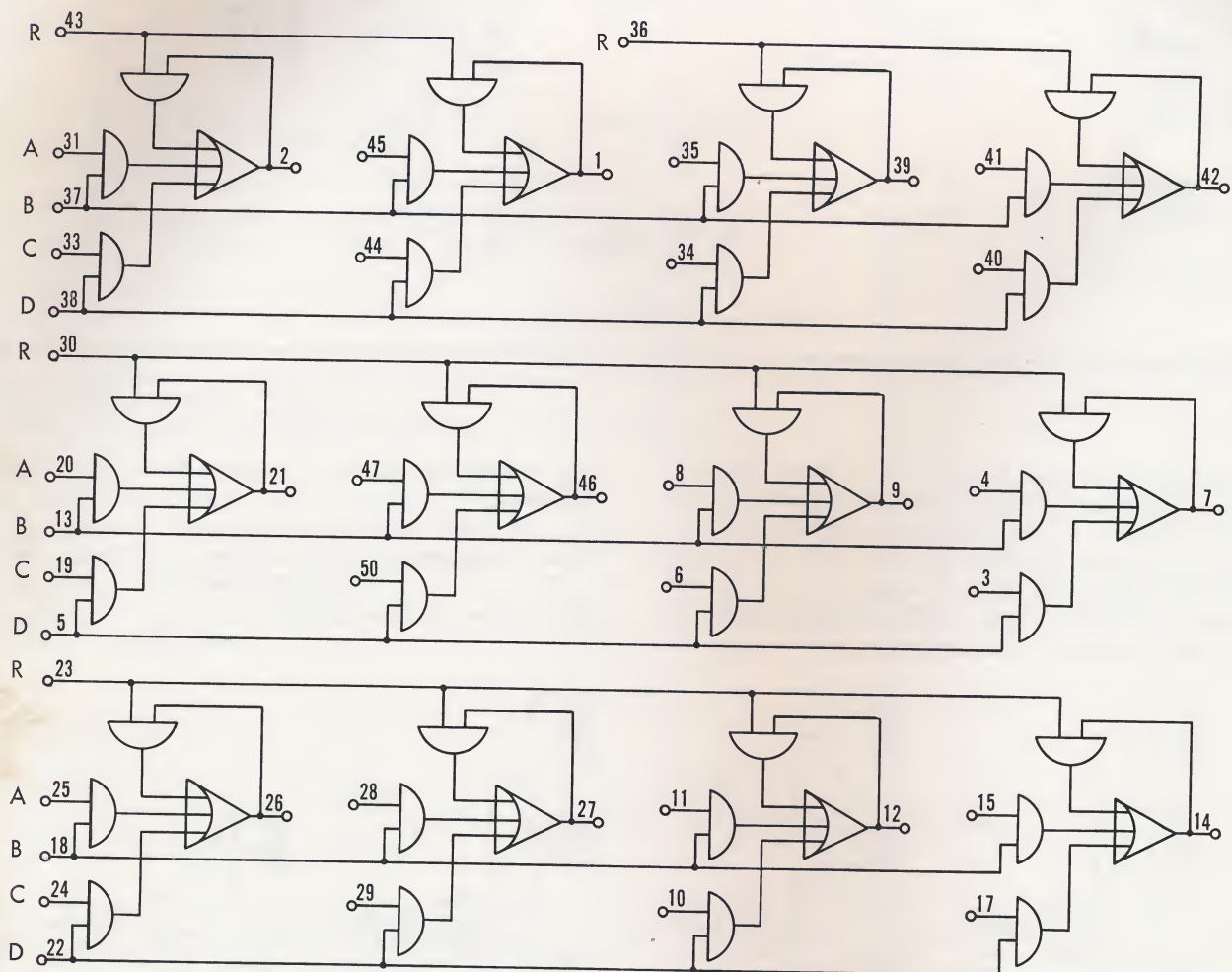
FT27 contains 12 latching circuits for use as unlocked storage elements. Each latch circuit has two gated inputs shown in the diagram below as $A \cdot B + C \cdot D$. B and D are each common to 4 latches and can be used as common control lines. Input R is the latching input. When R is True and $A \cdot B$ or $C \cdot D$ is True, the buffer output goes True and remains True until R goes False. This circuit provides a low cost

memory capability and can be used in applications where the fully buffered output of the T Series flip-flop is not required.

Power Requirements: +4v: 142 ma av., 189 ma max.

+8v: 122.4 ma

Dissipation: 1.74 watts max.



LOGIC DIAGRAM, FT27

LT10

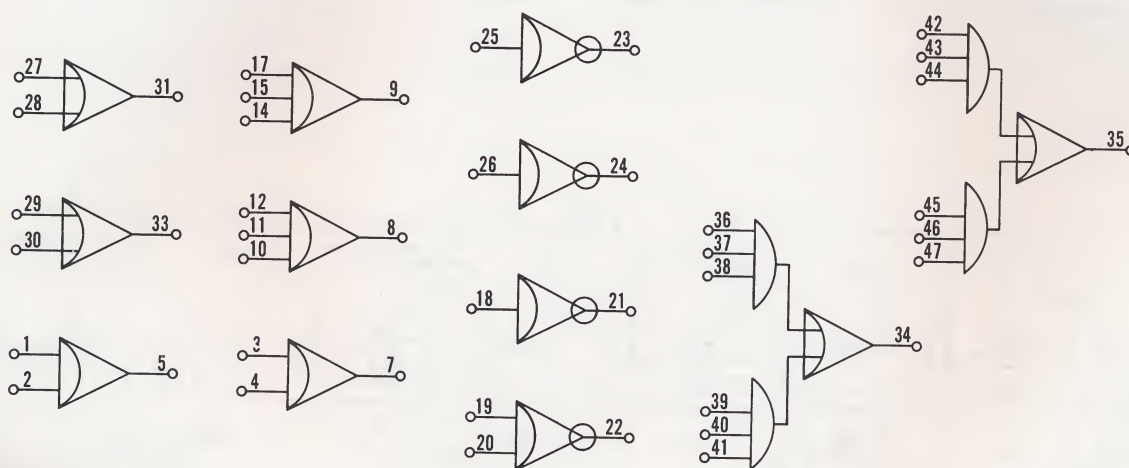
LT10 holds several general purpose elements in a useful assortment. The mixture includes 2 Buffered AND/OR gates in which each AND gate has 3 input terms; two 2-input Buffered OR gates; two 3-input Buffered AND gates; two 2-input Buffered AND gates; one 2-input NAND gate and 3 inverters. Each input represents one unit load, and each

LOGIC ELEMENTS, MODEL LT10

output can drive 14 unit loads.

Power Requirements: +4v: 127 ma av., 189 ma max.
+8v: 54.4 ma

Dissipation: 1.20 watts max.



LOGIC DIAGRAM, LT10

LT11

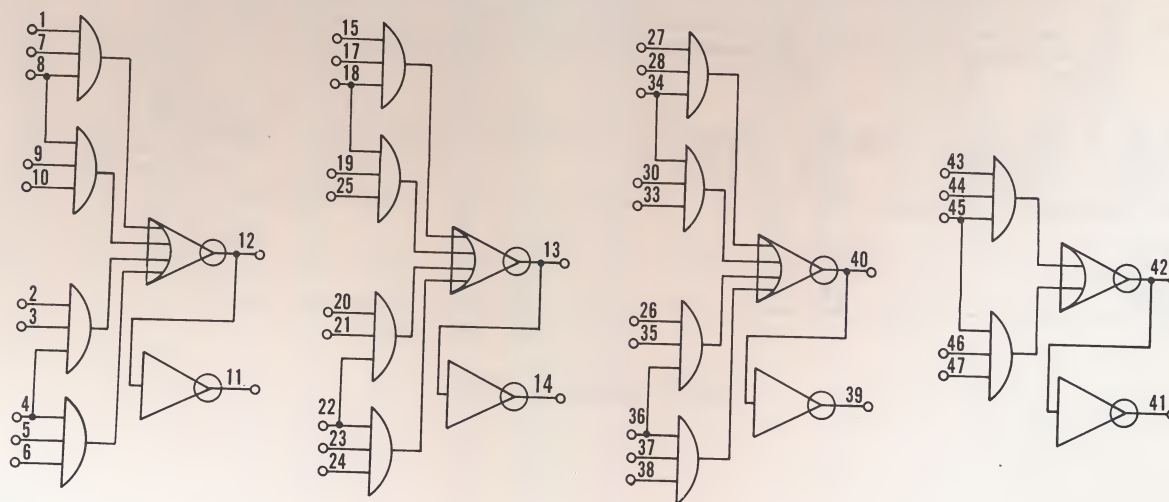
LT11 has four sets of gates arranged in an AND/OR form, especially suited for selecting sets of bits (in four bit "bytes"), and for forming parallel adders or subtractors, comparators, parity bit generators, and parity bit error detectors as well as many others. Each output has both true and false outputs available. One module can form a parity bit from an 8-bit parallel input, or detect a parity error from

LOGIC ELEMENTS, MODEL LT11

up to 9-bit inputs, or can compare the equality of two 7-bit words.

Power Requirements: +4v: 63 ma av., 126 ma max.
+8v: 61.2 ma

Dissipation: 0.99 watts max.



LOGIC DIAGRAM, LT11

8-VOLT INTERFACE BUFFERS, MODEL NT10; 8-VOLT INTERFACE INVERTERS, MODEL NT11

NT10/NT11

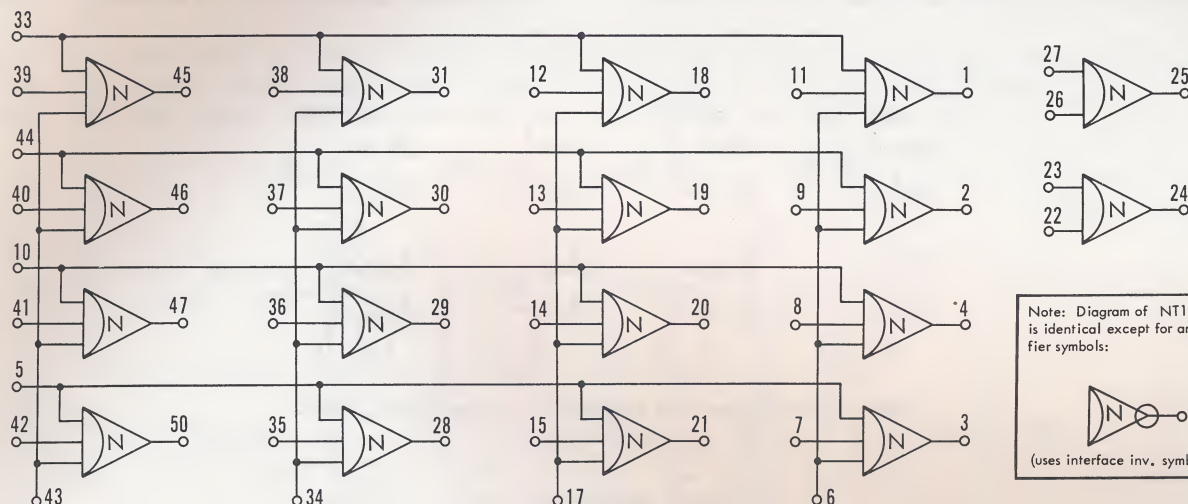
NT10 contains 2 BANDs and a 4 x 4 matrix of 3-input BANDs. All use standard T Series 0v/+4v input levels. Output levels are 0v and +8v. This module serves as interface from T Series to many other Positive True logic systems which use a high level of about +8v. Input tolerance is often sufficient to permit interfacing with 0v/+6v logic. Standard logic wiring may be used for interfacing provided

wire length is under 5 feet. NT11 outputs are inverted.

Output Current: 53 ma per driver

Power Requirements: +4v, 132 ma av., (NT10),
88 ma av., (NT11), 175 ma max.
+8v, 176 ma

Dissipation: 2.11 watts max.



LOGIC DIAGRAM, NT10

T SERIES TO NEGATIVE LOGIC INTERFACE, MODEL NT17

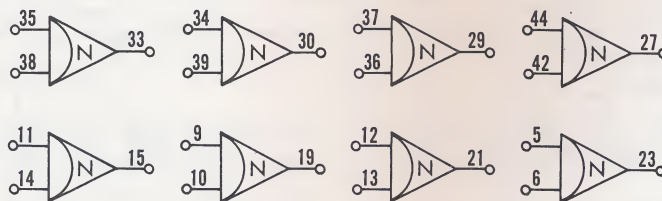
NT17

The Model NT17 contains eight 2-input AND gates which accept standard T Series 0v/+4v logic level input and drive 0v/-v output. The negative voltage, -v, represents logic 1 on the output, while 0v represents logic 0. Up to -12v can be supplied to the circuits from an external source for use as a negative logic level.

Output Current: 20 ma min. over the range -3v to -12v

Power Requirements: +4v, 16 ma av., 32 ma max.
+8v, 29 ma

-v, 51.6 ma av., 206 ma max. (pin 26)
Dissipation: 542 mw av., 3.83 watts max.



LOGIC DIAGRAM, NT17

NT18

The Model NT18 contains eight 2-input AND gates which accept 0v/-v input and convert to standard T Series 0v/+4v output. On input, the negative voltage, -v, becomes +4v output (logic 1) while input 0v becomes output 0v (logic 0).

Maximum negative input voltage is -12 volts. Either of two switching values may be used, as determined by a jumper

NEGATIVE LOGIC TO T SERIES INTERFACE, MODEL NT18

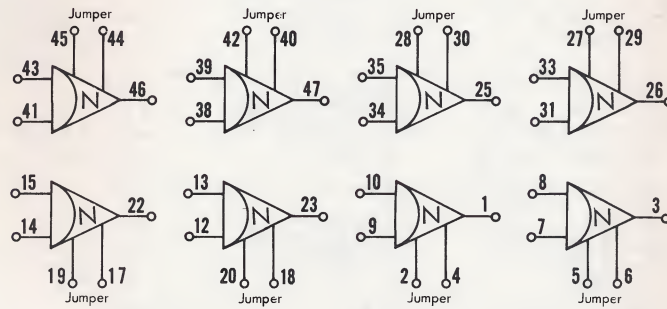
wire: -1.5v or -3v. When input logic level exceeds -4.5v, the -3v switching value should be used.

Input Current: -3v to -12v, 4 ma

Power Requirements: +4v, 120 ma av., 130 ma max.

-8v, 65 ma av., 100 ma max.

Dissipation: 1.0 watts av., 1.3 watts max.



Note: Add jumper wire to obtain -1.5v switching point.

LOGIC DIAGRAM, NT18

OT17

OT17 contains 4 one-shots with continuously adjustable output of pulsewidth 100 nsec to 100 μ sec. One of 7 ranges is chosen with jumpers. Minimum input pulse is 50 nsec True. Leading edge of output pulse starts typically 30 nsec after trailing edge of input pulse reaches nominal +2v switching value. Duty cycle is 50%. One-shot may not be retriggered before end of duty cycle. A power supply

ADJUSTABLE ONE-SHOTS, MODEL OT17

regulator is provided on the module for additional timing stability.

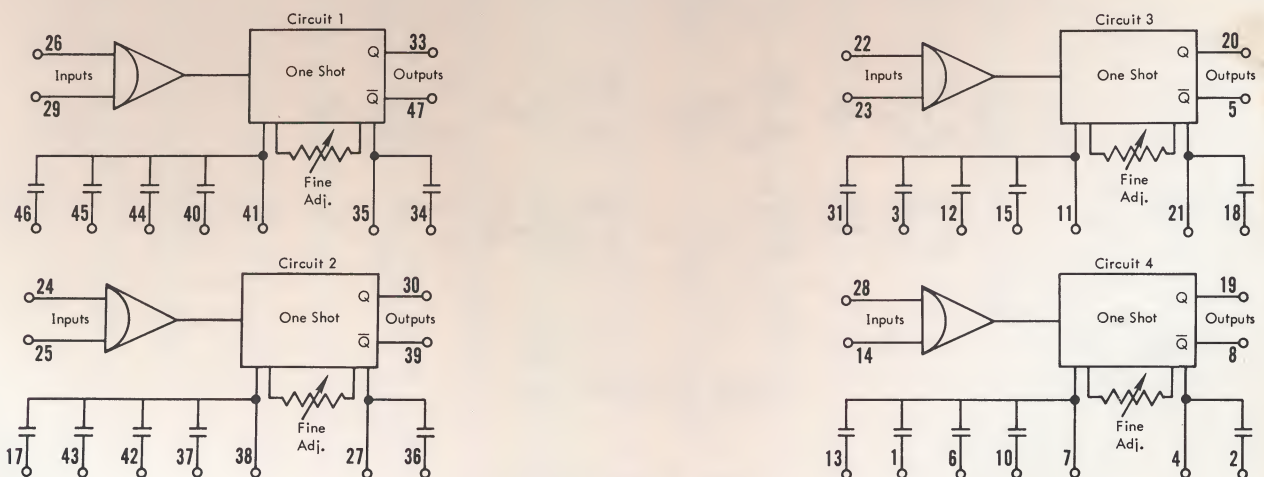
Pulsewidth range: 100 nsec to 100 μ sec, $\pm 10\%$

Fan-out: 14 unit loads per output

Power requirements: +4v, 125 ma

+8v, 330 ma

Dissipation: 3.15 watts max.



LOGIC DIAGRAM, OT17

LAMP DRIVERS, MODEL QT14; RELAY DRIVERS, MODEL RT14

QT14/RT14

QT14 and RT14 modules have 12 circuits, each circuit capable of switching an externally supplied load of 200 ma at voltage up to +28 volts. Every circuit has a 2-input buffered AND gate; one term is common with all other circuits on the module for common control. The boards have front-edge contacts for use with ET11 connectors and 14-conductor cable.

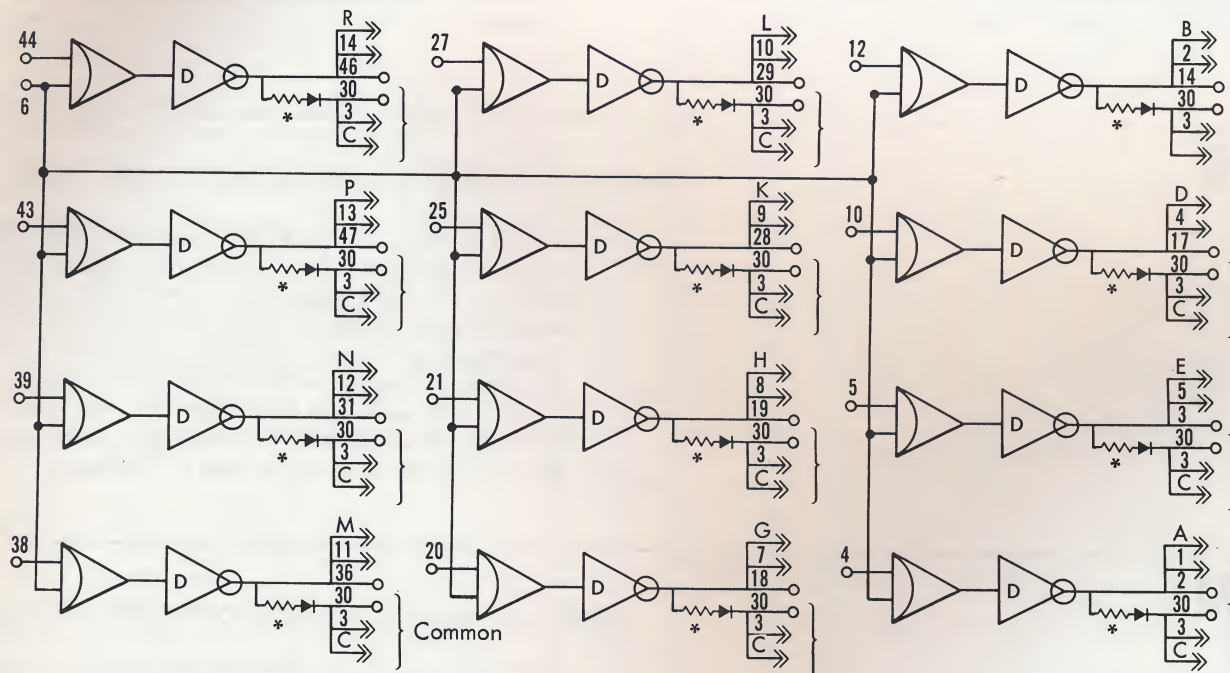
Each QT14 driver has a keep-warm resistor to prolong lamp life. These tie to common ground, through diodes, to minimize noise. The diodes protect the drivers from overload.

Each RT14 driver has a diode for peak inverse voltage protection, to be connected across the relay coil. In this case the common return is tied to relay +v.

Output rise and fall times are slowed to minimize noise. Maximum operating frequency depends on lamp or relay response time since this is usually the limiting factor.

Power Requirements: +4v, 268 ma av., 535 ma max.
+8v, 40.8 ma.

Dissipation: 2.47 watts max.



*Logic diagram for Model RT14 is identical except resistor is not present.

LOGIC DIAGRAM, QT14

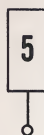
TERMINATOR MODULE, MODEL XT10

XT10

The XT10 module has forty-six 220 ohm resistors returned to +4v. They are used as line terminations for back panel wiring. Each terminator uses 5 unit loads of the driving circuit's fan-out. A maximum of 2 terminators may be used with one driver output, connected to the ends of two driven lines. No more than 1 terminator may be connected to one driven line. The terminators are required to achieve high propagation speeds and minimize signal reflections when logic lines are long. They need not be used when lines are short or when lower propagation speeds are acceptable.

Detailed wiring rules, and delay formulas, are given in Application Bulletin No. 64-51-04B.

Power Requirements: +4v, 414 ma av., 828 ma max.
Dissipation: 1.65 watts av., 3.30 watts max.



Of the 52 pins on the module, all are individually connected to terminators except 16, 32, 48, 49, 51, and 0.

ZT10

EXTENDER MODULE, MODEL ZT10

ZT10 has straight-through etch and a plug-in receptacle on its front edge. It permits the user to extend any module in front of the rack so that circuit operation may be investigated while the module is plugged into the rack. Contacts are Rhodium plated for long life.

ZT11

BLANK MODULE, MODEL ZT11

ZT11 has etched-circuit back-panel connectors. The remainder of the card is blank, for building circuits as desired.

ZT15

CABLE PLUG MODULE (SOLDER CONNECTIONS), MODEL ZT15

ZT15 will accept up to 44 shielded conductors: one 30-conductor cable and one 14-conductor cable, which are bolted to the front edge with a plastic cable clamp. All conductors and shields should be soldered to etch provided. Extra mounting holes and interconnecting etch are provided for cable termination network component mounting. The ZT15 is most useful for low-frequency work (under 1 Mc) where the effects of parasitic capacitance are not important and noise levels need not be kept to a minimum.

ZT23

CABLE PLUG MODULE (PRESSURE CONTACTS), MODEL ZT23

ZT23 will accept up to 28 shielded conductors, as two 14-conductor cables, which are connected to etch terminals on the module front edge by means of ET11 cable connectors (see Accessories). The etch runs straight through from front-edge to back-panel pins, with no provision for mounting of other components. The ZT23 is most useful where interconnection impedances must be carefully controlled.

ZT37

BREADBOARD MODULE, MODEL ZT37

ZT37 has a versatile etch circuit pattern arranged for convenient mounting of all standard components, including diodes, capacitors, resistors, 14-lead dual in-line flat-packs, and transistor or IC TO-5 cans. This module permits custom building of special circuits while retaining the advantages and mechanical compatibility of T Series etch circuit construction.

T SERIES INTEGRATED CIRCUITS

Three standard integrated circuit types account for 90% of the active circuits in a typical T Series system. They are a buffer (4 per chip), an inverter (4 per chip), and a flip-flop (1 per chip). They are mixed with discrete component gates and pull-up resistors.

The apparently incompatible goals of low cost and logic flexibility are simultaneously achieved in T Series by integrating the complex portion of each logic circuit but retaining the more simple gating structure in discrete component form. The logic designer can now use natural logic: AND, OR, NAND, NOR functions are available in a large assortment of gate configurations, all using the same standard I. C. buffers and inverters for economy. The simplified buffer schematic, below, shows a typical mix of discrete with integrated circuits. Greater logic flexibility at lower cost is the result.

High current drive without loss of equipment reliability is another benefit derived from mixing standard I. C. 's with discrete components. Most dissipation takes place outside the I. C. chip. This permits current drive of 60 ma per output as compared with the typical 15 ma available from off-the-shelf fully integrated circuits. The additional current and additional component precision allows fan-out of 14, compared to the typical 8 of other module lines. This reduces the amount of logic circuitry and provides enough power to drive longer logic lines, indicator lamps, and in many cases cabling as well. Increased speed with

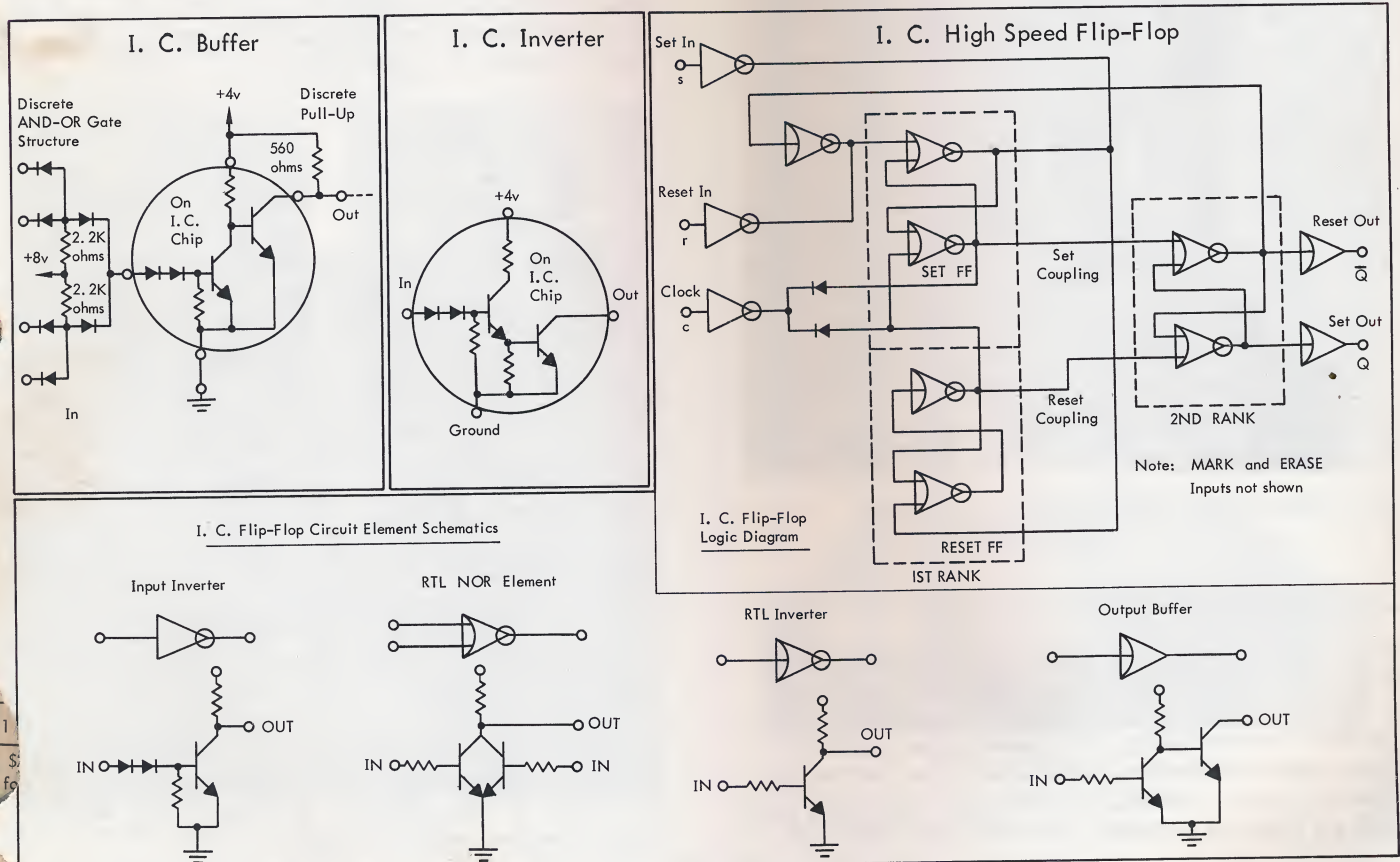
less hardware is the result.

A third benefit is operation at higher switching voltage, made possible by having gate pull-up voltage higher than logic level voltage. The switching point is placed at +2 volts, an ideal value for noise rejection.

FLIP-FLOP OPERATION

The integrated circuit flip-flop, shown below, is a dual rank configuration of RTL NOR elements. The 2nd rank is a simple NOR latch coupled to the output pins through buffers that each provide 60 ma output current. The first rank consists of two flip-flops, one for set and one for reset. The two lines which couple the second rank to the first rank also connect to the clock inverter. When the clock goes high these two lines are clamped to ground isolating the second rank so that it retains its initial state. During the period that the clock is high the set and reset flip-flops are primed to the state of their inputs. When the clock falls they are allowed to assume the new states and regain control of the second rank flip-flop. The outputs change to the new state on the trailing edge of the clock. Inputs must be True for 30 nsec preceding and 5 nsec following the clock trailing edge.

The second rank output is fed back to the first rank so that the outputs remain unchanged when clock pulses occur with both set and reset inputs False. Note that the set inverter will always override inputs to the reset inverter when the set input is True.



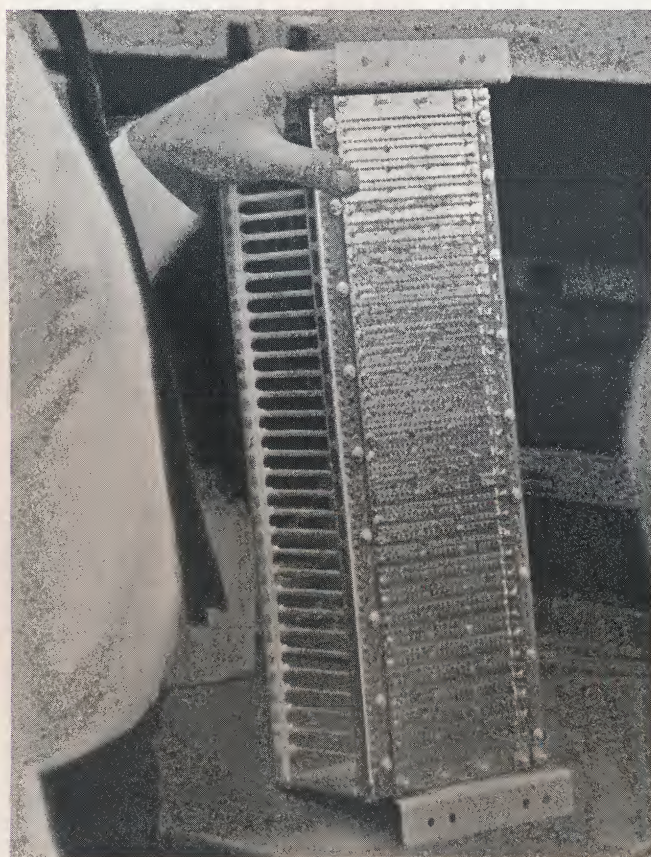
ACCESSORIES

MOUNTING CASES AND ASSOCIATED HARDWARE

Standard cases accommodate 32 modules, are 5-1/4 inches high, and fit into a standard 19-inch width rack. Wiring terminals can be either solder-tail or wire-wrap. Each case comes with connectors, +4v and +8v power wiring, and ground plane installed. Brackets are adjustable.

Standard Mounting Cases

1. Solder terminals, fixed mount: MT10
2. Solder terminals, vertical hinge, right or left: MT30
3. Wire-wrap terminals, fixed mount: MT12
4. Wire-wrap, vertical hinge, right or left: MT32



MT12 Fixed Mount Case, Showing Ground Plane

High-Density Drawer Type Mounting Cases

Model MTD1 mounting case holds up to 90 modules, is 8-3/4 inches high, and fits into a standard 19-inch rack. It has full-extension tilt slides, and comes with connectors, +4v and +8v power wiring, and ground plane installed. Panel-mounted indicators and switches can be mounted behind front panel. Model ZT20 blower and removable, washable air filter are included. Terminals are solder-tail.

Model MTD2 mounting case is similar to MTD1, but has wire-wrap terminals in place of solder-tail.

Blower

Model ZT20 blower assembly contains three muffin-fans side by side in a housing 19 inches wide by 7 inches deep by 1-3/4 inches high. Its capacity is 300 cfm.

Jumper Kit

Model VT10 jumper kit contains an assortment of 500 slide-on jumper wires. This approach offers significant improvements in reliability and convenience over taper pin techniques. The terminals at the ends of each wire slide on wire-wrap pins. Terminals may be stacked two high on each pin. Wire is No. 24 AWG stranded copper with white polyethylene insulation. Wire lengths within each kit are:

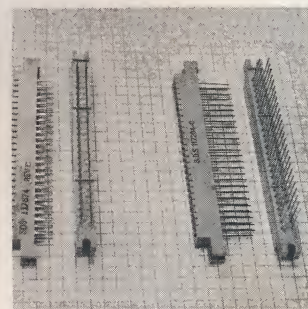
Quantity	Length	Quantity	Length
80	1.0"	30	10.0"
100	2.2"	20	12.0"
100	3.3"	15	15.0"
100	4.7"	10	18.0"
40	6.8"	5	27.0"

Connectors

Model VT11 wire-wrap connector and VT12 solder-tail connector are identical to those used in the MT mounting cases. They are useful for special installations.



VT10 Jumper Kit



VT11 and VT12 Connectors

Indicator Lamp And Socket

Model ZT39 miniature incandescent lamp mounts on a panel through a 5/16 inch hole with mounting clip (socket) provided. Wires can be soldered or wire-wrapped to the lamp or connected with push-on jumpers. Lens is translucent white.

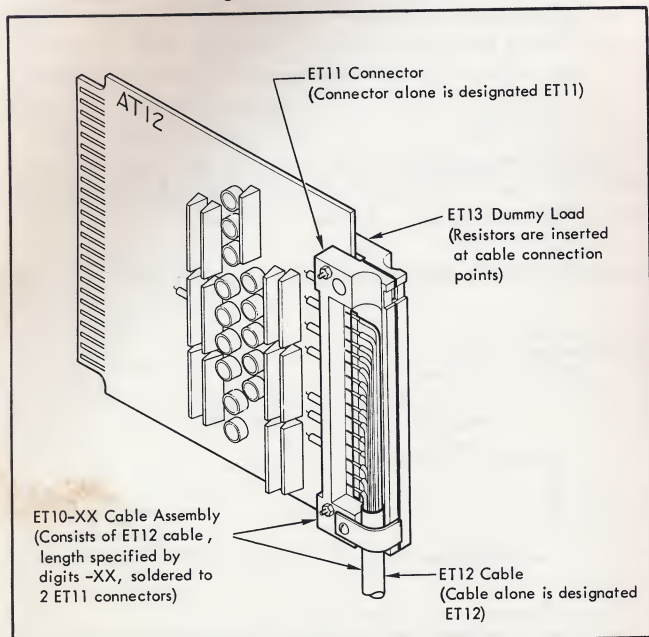
The lamp can be driven directly by any T Series standard 0v/+4v logic level output. It draws 48 ma at +4v, or 13 unit loads. At this voltage the ZT39 has a life of 480,000 hours, or approximately 5.6 years.

CABLING COMPONENTS, ET10, ET11, ET12, ET13

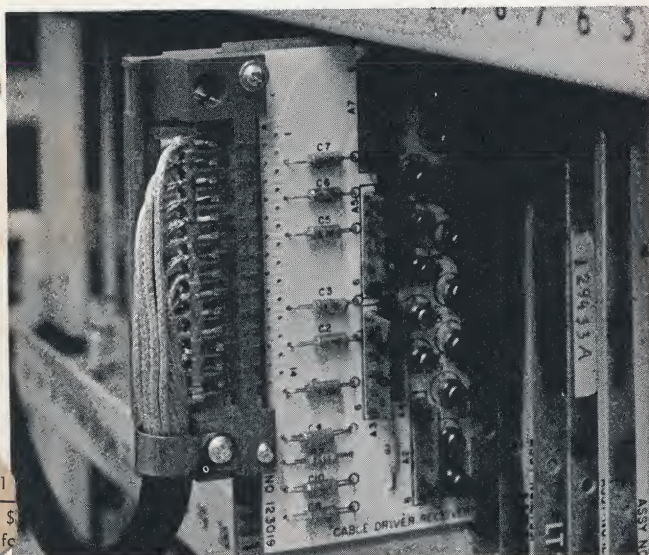
ET cabling components include the following:

1. ET11 connector, bolts to one side of front edge of AT10, AT11, AT12, QT14, RT14, and ZT23 modules. Accepts ET12 cable.
2. ET12-XX* cable, 14 conductor shielded, cut to specified length (up to 100 feet).
3. ET13 dummy load, required when only one 14-conductor cable is attached to an AT10, AT11, or AT12 module.
4. ET10-XX* cable-connector assemblies; consist of two ET11 connectors soldered to both ends of a length of ET12 cable.

*XX defines length in feet; specify when ordering.



ET Cabling Components



ET10 Assembly Mounted On AT11 Module

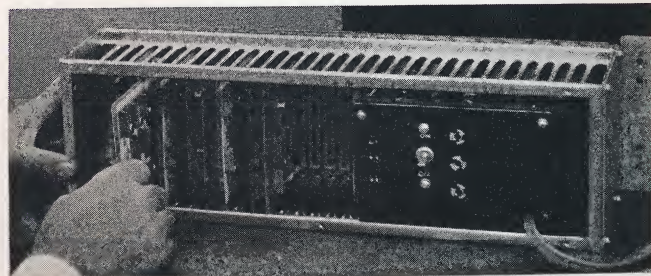
POWER SUPPLIES

Model PT10 Compact Supply

Model PT10 fits into an MT10, MT30, MT12, or MT32 mounting case, occupying 15 slots. It can power from 35 to 55 modules depending on load. Included are output voltage adjustments and protection against short circuits and overvoltage.

Input: 50 to 400 cps, 1 ϕ , 110 vac to 230 vac

Outputs: +4vdc, 10 amp.
+8vdc, 2 amp.
-8vdc, 0.2 amp.
22vac, 1/2 amp.



PT10 Compact Power Supply Installed Beside Logic Modules

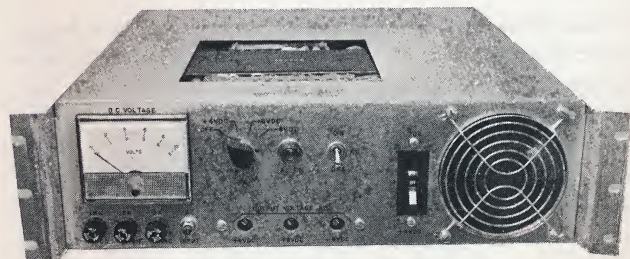
Model PT12 High Power Supply

Model PT12 handles higher power applications. It occupies the full 19-inch rack width, is 5-1/4 inches high and 22 inches deep. Front panel has a cooling fan, removable, washable air filter, on-off switch, multi-range switched voltmeter, and pilot light. Included are output voltage adjustments, short circuit and overvoltage protection, and remote sensing.

Input: 47 to 63 cps, 1 ϕ , 115 vac, 127 vac, 208 vac, or 220vac

Outputs: +4vdc, 60 amp.
+8vdc, 12 amp.
-8vdc, 1.8 amp.
25vac, 4 amp.

(Regulation $\pm 5\%$ on all outputs)



PT12 High Power Supply

III. ELEMENTS OF LOGIC DESIGN

INTRODUCTION

This section presents some basic principles of logic design. It is written for the technically trained person who is not familiar with logic design concepts, or who desires a brief review. Enough information is presented to enable the reader to design simple control and processing circuits using SDS T Series modules. Additional information is available in T Series Application Bulletins.

These topics are covered:

1. Logic Fundamentals and Elementary Boolean Algebra.
2. Operation of T Series Logic Circuits: decision elements (gates), amplifiers and inverters, and clocked storage elements (flip-flops).
3. Implementation Techniques: planning the machine, deriving Boolean equations, and mechanizing equations with hardware.

LOGIC FUNDAMENTALS AND BOOLEAN ALGEBRA

BINARY LOGIC

Digital logic elements which operate with two distinct states are called binary elements. The two states are named True and False, on and off, or 1 and 0. In electrical equipment they are most often two voltage levels. One voltage level is always more positive (or less negative) than the other, and is called the high level, the other the low level. If the high level is defined as logically True (1), and the low level as logically False (0), the logic is called high level logic. Low level logic is the opposite. If the True (high) level of high level logic is a positive voltage, such logic also is referred to as positive true.

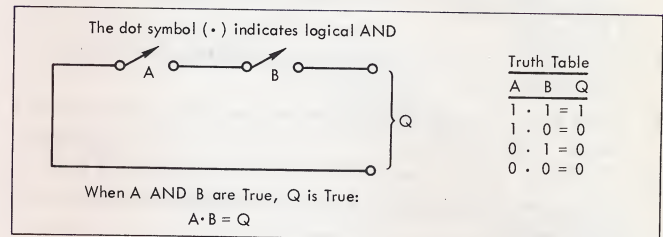
T Series circuits employ positive true logic: a +4 volt level is defined as True (1) and a 0 volt level is defined as False (0).

BOOLEAN ALGEBRA

Because of the similarity between classical logic and binary electronics, Boolean algebra, the mathematics of logic, is applied to the design of binary electronics. The algebra uses alphabetic symbols to represent logical variables and 1's and 0's to represent states. Three fundamental logic operations, AND, OR, and negation are the basic operations of this algebra.

An electrical contact switch is an easily understood binary device which can be used to demonstrate logic concepts. For the following discussion an open contact is defined as logical 0, or False (does not allow current to flow), while a closed contact is defined as logical True (1).

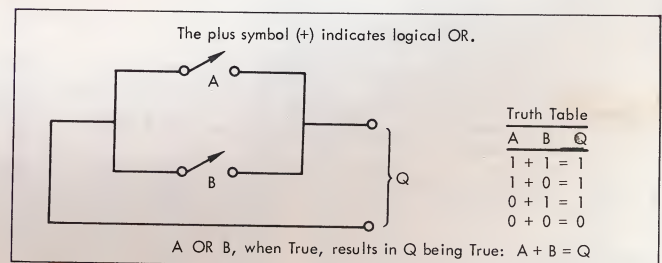
Logical AND



The combination of switches is called an AND gate. The output is True (current flows) only when A AND B are both True. The truth table expresses all possible states of the two inputs (A, B) and the corresponding output for each input combination. The first line of the table states that when both contacts are closed (1•1) current flows (Q = 1). The other three lines state that no current can flow (Q = 0) when either one or both contacts are open.

The dot symbol is often omitted for convenience: $A \cdot B = AB$.

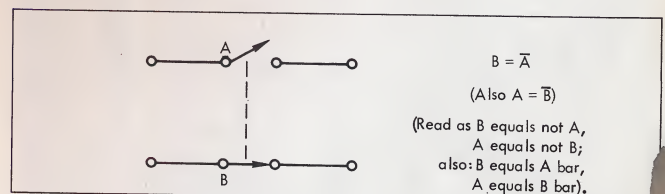
Logical OR



Inspection shows that the OR gate output is True when either A OR B OR both are True.

Logical Negation

The bar symbol over a variable ($\bar{}$) indicates logical negation or inversion. If two contacts are arranged so that one is always open when the other is closed, and vice versa, then one is called the logical complement of the other.

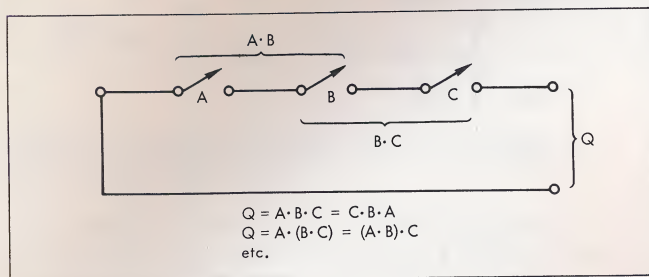


The opposite state of a single contact is also its complement: for instance, $\bar{A}$ is the complement or inverse of A.

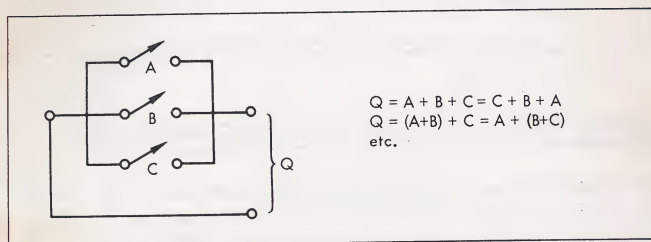
Additional Variables

These fundamental operations can be combined into more complex groupings and extended to more variables.

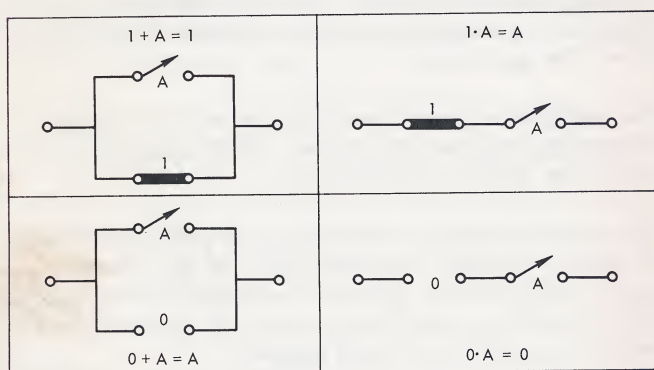
The AND function may be extended by adding more switches in series. Inspection shows that the order or grouping of terms does not affect the end result:



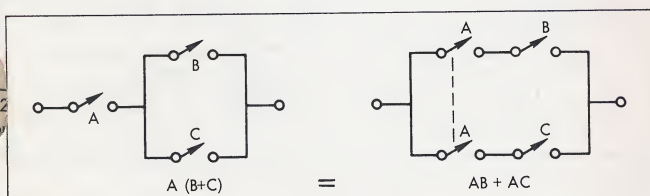
Similarly, the OR function may be extended by adding more switches in parallel:



Identities may be demonstrated in like manner:



AND and OR functions may also be combined:



Simplification Theorems

These relationships, and others, are summarized in a set of theorems which are used to reduce complex logic networks to a minimum of terms. They may all be demonstrated with switch diagrams or truth tables.

1. Identities

$$\begin{aligned}
 A + A &= A \\
 A \cdot A &= A \\
 A + \bar{A} &= 1 \text{ (always True)} \\
 A \cdot \bar{A} &= 0 \text{ (always False)} \\
 A + 1 &= 1 \\
 A + 0 &= A \\
 A \cdot 0 &= 0 \\
 A \cdot 1 &= A
 \end{aligned}$$

2. Commutative law

$$\begin{aligned}
 A \cdot B &= B \cdot A \\
 A + B &= B + A
 \end{aligned}$$

3. Associative law

$$\begin{aligned}
 A \cdot (B \cdot C) &= (A \cdot B) \cdot C \\
 A + (B + C) &= (A + B) + C
 \end{aligned}$$

4. Distributive law

$$\begin{aligned}
 A \cdot B + A \cdot C &= A(B + C) \\
 (A + B) \cdot (A + C) &= A + (B \cdot C)
 \end{aligned}$$

5. Absorption: $A \cdot (A + B) = A$

6. $A + \bar{A}B = A + B$

7. DeMorgan's Theorem: To complement a Boolean expression, complement each character in the expression and interchange the AND and OR functions throughout.

Examples:

$$\begin{aligned}
 \text{Complement } \bar{A}: & \quad \overline{(\bar{A})} = A \\
 " \quad A + B: & \quad \overline{(A + B)} = \bar{A} \cdot \bar{B} \\
 " \quad A \cdot B: & \quad \overline{(A \cdot B)} = \bar{A} + \bar{B}
 \end{aligned}$$

Proof By Truth Table

The truth table provides a useful method of proving logic theorems and simplifying equations by providing a means to test the validity of any logic equation.

As an example, prove the validity of $\overline{A \cdot B} = \bar{A} + \bar{B}$. First, make a column for each variable involved and enter enough rows of binary values to cover all possible combinations of the basic variables (columns 1 and 2, below). Then form the additional columns needed to define all values of the terms in the equation to be verified (columns 3 through 7).

Column No.:	1	2	3	4	5	6	7
Variable:	A	B	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A}$	$\overline{B}$	$\overline{A+B}$
All possible combinations of two variables, A, B	0	0	0	1	1	1	1
	0	1	0	1	1	0	1
	1	0	0	1	0	1	1
	1	1	1	0	0	0	0

note that these are identical

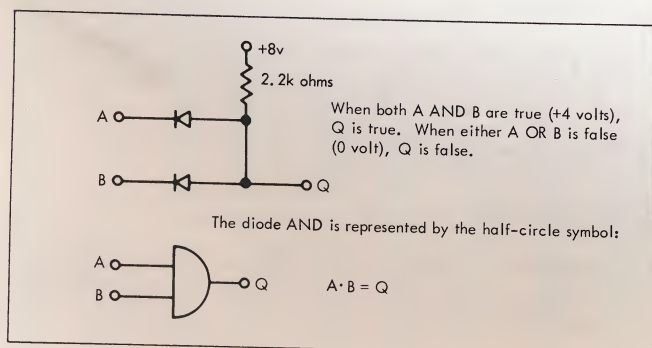
The identity of columns 4 and 7 shows that the function $\overline{A \cdot B}$ is equal to $\overline{A+B}$, thus proving this example of DeMorgan's theorem. This technique is very powerful because it is universally applicable, and can be used to test the validity of any proposed Boolean equality.

OPERATION OF ELECTRONIC LOGIC

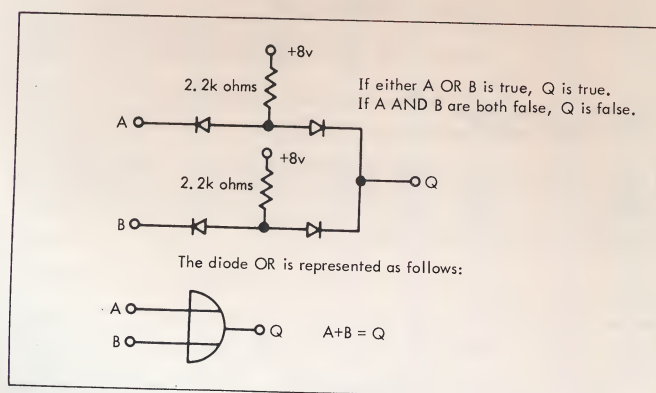
DECISION ELEMENTS (GATES)

T Series uses diodes to perform the switching functions (decisions) as described below.

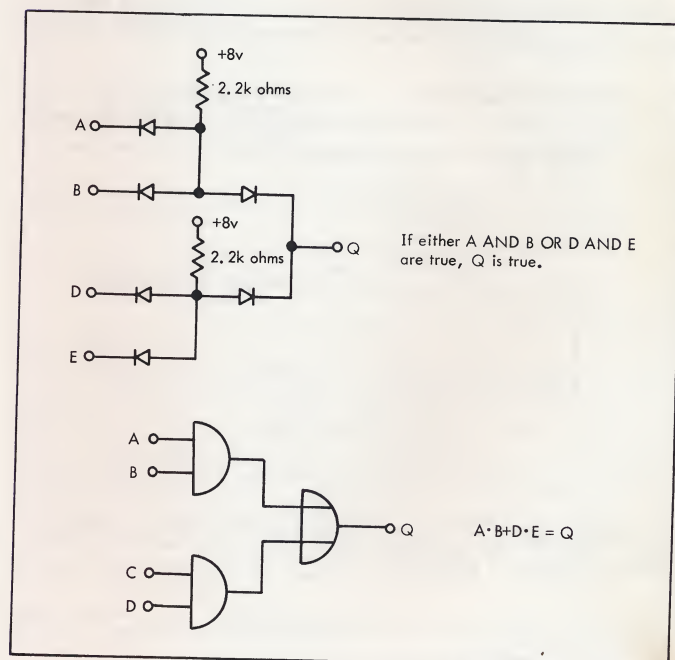
Diode AND



Diode OR



Diode AND and OR Gates Combined (AND/OR Gates)

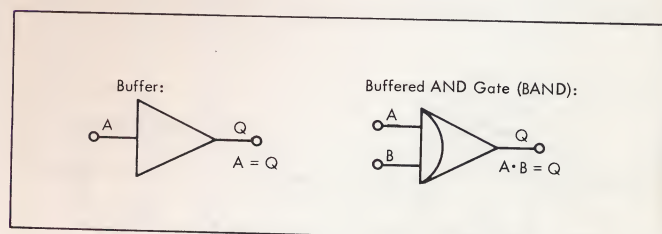


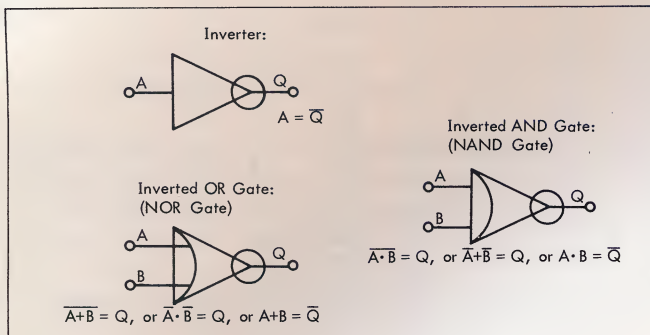
BUFFER AMPLIFIERS AND INVERTING AMPLIFIERS

In order to preserve good signal characteristics, the output of a diode AND, OR, or an AND/OR combination never serves as input to another stage of diode gate circuits, but is always connected to an active element, which restores the signal to the proper power level and filters out random noise. Active elements include inverting amplifiers, non-inverting (buffer) amplifiers, flip-flops, and some special circuits. The outputs of these active elements may then drive other gate inputs.

The most basic active elements are the amplifiers, which standardize the signal waveshape, and provide power gain for driving parallel loads (fan-out).

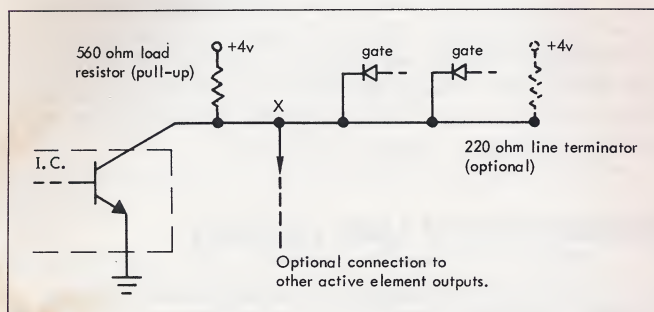
The inverting amplifiers also perform the additional function of logical negation. The circle shown on the inverter symbol indicates this. The non-inverting amplifiers, called buffer amplifiers, provide power gain and signal level correction but perform no logical function.





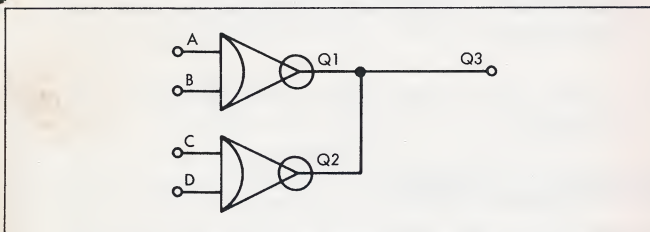
LOGIC FUNCTIONS FORMED BY CONNECTING ACTIVE ELEMENT OUTPUTS

Buffer amplifiers, inverters, and flip-flop integrated circuits all have the same output element. It is a transistor whose output drives the logic line:



When other output transistors are connected at point X, an AND function is formed. If any one transistor conducts it shorts the logic line to ground, placing the line at logic 0. This is an AND function because all outputs must be logic 1 if the line is to be at logic 1.

If all outputs are inverter outputs, this function may also be thought of as a NOR. Consider two NAND gates:



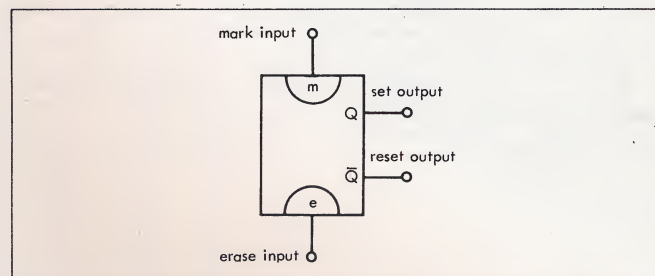
Output $Q1 = \overline{A \cdot B}$, and output $Q2 = \overline{C \cdot D}$. By connecting Q1 and Q2 an AND function is formed, $Q3 = \overline{(\overline{A \cdot B}) \cdot (\overline{C \cdot D})}$. By DeMorgan's theorem, this is equivalent to $Q3 = \overline{(\overline{A \cdot B}) + (\overline{C \cdot D})}$ which is a NOR function because it has the form $Q = \overline{X+Y}$ (where $X = A \cdot B$, $Y = C \cdot D$).

STORAGE ELEMENTS (FLIP-FLOPS)

The preceding described how gate elements can be used to make logical decisions. The results of any gating decision must often be retained for some period of time, even though the conditions that caused the decision are removed. The element most commonly used in conjunction with gates to store a decision is the flip-flop. This element has two stable states. It is on or set in one state, and off or reset in the other. Signals applied to the inputs of a flip-flop control the state it is in. Once the flip-flop has been placed in either state, it will remain so until purposefully changed. Thus the flip-flop has memory.

DC Flip-Flop Operation

A simple, unlocked flip-flop with gates connected to inputs is shown below. This is often called a dc flip-flop, and in T Series nomenclature the dc inputs are given the designations mark (m) for dc set input, and erase (e) for dc reset input.



When the mark input becomes True, the set output becomes True and stays True regardless of the state of the mark input, and the reset output becomes False. When the erase input becomes True, the reset output becomes True and stays True, and the set output becomes False. If both dc inputs become True simultaneously, both outputs will become False as long as both inputs are held True. If one input then becomes False the flip-flop assumes the state determined by the other input.

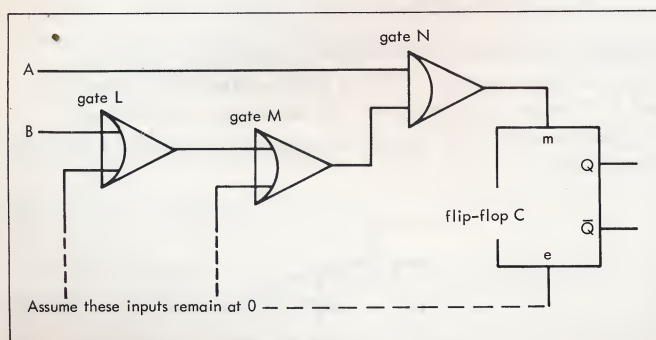
Clocked Flip-Flop Operation

It is often advantageous to provide an additional timing pulse, called a clock, which provides a time reference throughout the system. This clock controls the point in time when the results of a logic decision should be used to set or reset a flip-flop.

Clocked logic avoids timing problems due to race conditions which can result when level changes arrive at flip-flop inputs at different times, because of different propagation delays in the electrical components in parallel paths leading to the same flip-flop. A race condition is present when one signal causes a flip-flop to change state before all signals have had time to settle to their final levels.

As an illustration, consider the simple network shown on page 34. Assume that flip-flop C is initially in the reset

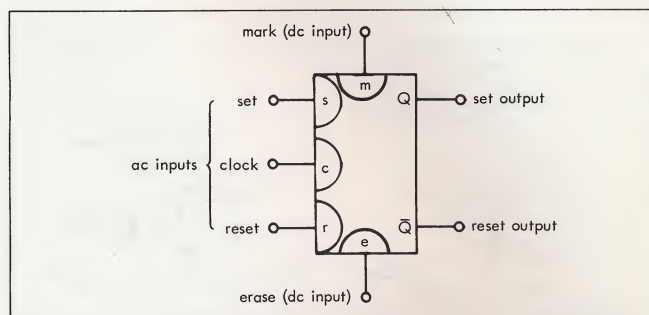
condition. Also assume that level A is initially 0 while level B is initially 1. Now if A goes to 1 and simultaneously B goes to 0, the new value of A arrives at gate N before the new value of B arrives, because the B change is delayed in going through gates L and M. Therefore, both inputs to gate N are True for the duration of the delay. Since the mark input of C is at all times sensitive to the output of gate N, flip-flop C will erroneously set if the delay is long enough. When the new value of B finally arrives at gate N, the desired input condition to flip-flop C is established, but an incorrect result has already been stored in C and cannot be reversed.



Clocking of flip-flop inputs avoids this type of problem. The function of the clock is to inhibit all flip-flop activity except during precisely timed periods. When all flip-flop and gate outputs have had time to reach their final states, the clock pulse enables the appropriate flip-flop inputs to accept the new levels, and the new decisions in the chain are correctly stored.

A number of clock pulse systems are in use, but the one which offers the greatest timing reliability with the least clock duty-cycle restriction is trailing-edge triggering. It permits a flip-flop to accept input signals only on the 1 to 0 transition of the clock pulse, which in T Series is a time period of about 10 nanoseconds duration. With this kind of clock trigger, flip-flop operation is relatively insensitive to either height or width of the clock pulse. When clock cycle is sufficient to permit all logic signals to settle, then race conditions are avoided. (See pages 6, 7, and 8 for further discussion of delay and timing).

T Series flip-flops have a pair of logic signal inputs for clocked operation (ac inputs) called set (s) and reset (r). The input for the clock pulse is designated c. Whereas the dc inputs, mark (m) and erase (e), respond directly to level changes, the ac inputs respond to level changes only during the 1 to 0 clock transition. Thus the dc inputs are useful only when there is no possibility of race conditions or when the logic designer has made provision to avert the effects of races. The diagram at right shows the complete T Series flip-flop symbol.



SPECIAL CIRCUITS

The basic elements described above are used to perform nearly all logic functions in digital systems. These basic elements are usually supplemented by several special circuits. An oscillator is required to generate the precise clock pulses. One-shot circuits can assume one state temporarily for a preset period before automatically returning to their previous state. Schmitt Triggers are level sensitive, pulse shaping devices used to convert various inputs to standard logic levels. Power amplifier circuits are needed for driving relay coils and indicator lights. These special circuits are described in detail in Section II.

IMPLEMENTATION OF LOGIC FUNCTIONS

In this section a knowledge of the binary number system is assumed.

PLANNING THE DEVICE

Before starting logic implementation the designer must clearly establish his goals. This is usually done with the aid of three basic design documents:

1. An input, output, and function specification.
2. A communication diagram (block diagram) showing the major function blocks with all signals between them identified.
3. A flow chart or state diagram which shows the sequence of events.

Description of an Example

The principles can be illustrated with a simple example.

The designer is asked to construct a machine that will recognize a given pattern in a string of binary signals arriving serially, and generate a prescribed set of output signals when, and only when, the desired input pattern is recognized. This is a typical problem that occurs when handling data from electronic equipment which monitors a physical process in a laboratory or production line situation. Similar problems

exist in telemetry, remote control of medical equipment, etc. Typically the input pattern might represent a danger condition and the prescribed output would cause corrective action to take place.

A simple, commonly used technique for transmitting a string of binary signals is to change the voltage level on one input at precisely timed intervals. The receiving device examines the input during each interval and registers a 0 or a 1, depending on whether the voltage is at the False or True level. The clock rate of the receiving device must be synchronized with the clock rate of the transmitting device. The input signal is thus recognized as a string of 1's and 0's occurring in sequence, such as 01100100011101....

In the example to be given, the machine is to recognize the pattern 10010, where the leading 1 is the first bit to arrive and is defined as the least significant bit (LSB), while the last 0 is the last to arrive and is defined as the most significant bit (MSB).

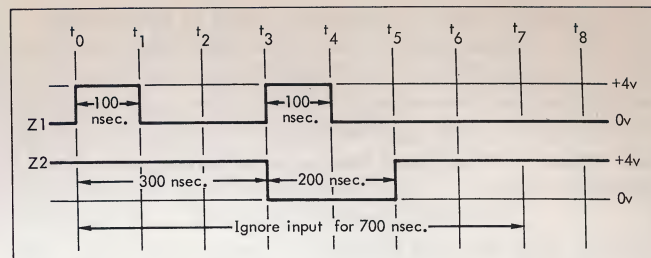
The Design Specification

The design specification is a concise, unambiguous statement of the problem. A sample design specification for this example is the following.

Construct an electronic device having the characteristics specified:

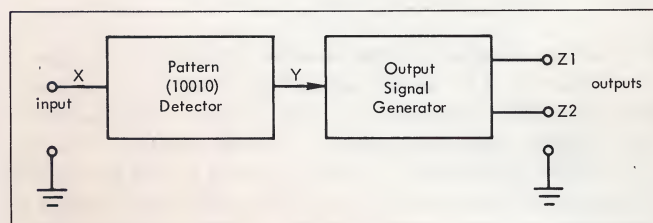
1. Functions to be performed. Recognize the pattern 10010 in a string of binary signals arriving serially, at a 10 Mc clock rate, at the input described in item (2). When this pattern is recognized, ignore all successive 10010 patterns which occur during a period of 800 nanoseconds after the trailing edge of the last bit in the pattern (MSB).
2. Input. The input signal, designated X, is a series of binary level changes between 0v, $\pm 1.5v$, (False) and $+4v$, $\pm 1.4v$ (True). The level changes are clocked at a 10 Mc rate; assume that the clock signal in the device to be designed is at all times synchronized with the clock in the transmitting device. The input signal may be received between any T Series gate input and ground.
3. Output. Generate logic signals at two terminals, Z1 and Z2, with timing relationships as shown in the diagram that follows, and with amplitudes of 0v (False) and $+4v$ (True). Outputs are to be taken from a T Series logic amplifier. Time t_0 is to occur one clock period after the trailing edge of the MSB.

Clock Signal. The clock signal in the device is to be set at a 10 Mc rate, and is to have characteristics appropriate for operation of T Series flip-flops (trailing edge triggering). It is synchronized with the clock signal that controls the input signal defined in item (2).

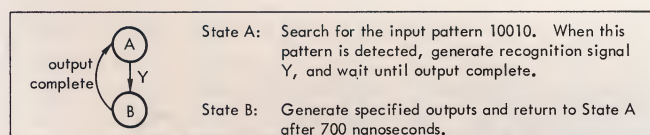


Block Diagram and Flow Chart

Two distinct functions are required: pattern recognition, and the generation of a prescribed output. Their functional relationship can be symbolized by a block diagram. The signal Y is defined as the signal which indicates that the pattern 10010 has been detected, and serves as input to the Output Signal Generator.



The required sequence of events and timing is expressed with a flow chart:



DERIVING THE PATTERN DETECTOR EQUATIONS

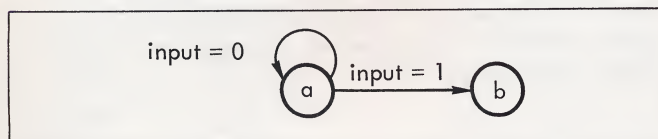
The two functions will be designed one at a time, the Pattern Detector first. The design technique used in this example is the Huffman-Mealy method,* which minimizes the number of storage elements (flip-flops) in the system. There are six steps in the solution of this type of problem: (1) identify the inputs and outputs; (2) determine all necessary internal states of the device, and relate them to inputs and outputs with a state diagram; (3) assign storage elements to the states; (4) using a truth table, derive input equations to the storage elements which will cause them to change state as required by the state diagram; (5) simplify the equations; and (6) derive and simplify the output equations.

When the equations have been reduced to simplest form the device may be implemented with hardware.

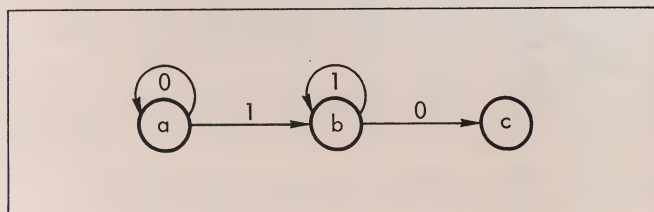
*For a thorough discussion of logic design methods see *The Logical Design of Digital Computers*, by Montgomery Phister, Jr. (John Wiley & Sons, 1959).

First, identify inputs and outputs. Input to the Pattern Detector is as specified in item (2) of the Design Specification. Output of the Pattern Detector is to be signal Y, which goes True immediately following the negative-going clock transition that signifies the trailing edge of the MSB, and returns to its original level one negative-going clock transition later.

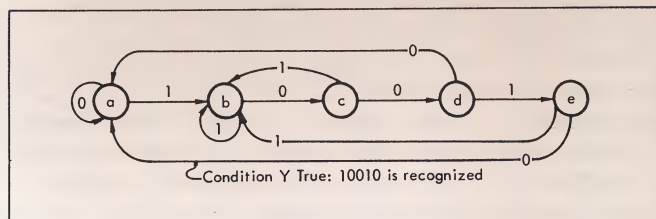
Second, draw the state diagram for pattern detection. Let the network be in state a initially (assume no previous input; that is, device has just been reset). If the first bit is a 1, let the network go to state b, indicating "recognition possible." If on the other hand input is logic 0, let network remain in state a, indicating "recognition not possible." These decisions derive from the fact that the pattern (10010) starts with a 1. Draw the diagram:



Proceeding as before, if the network is in state b and the next input bit is 0, let the network go to state c, indicating recognition possible (1 0 010); while if the next bit is a 1, let it remain in state b. (At first thought, the network might be expected to return to state a, but the second bit received could actually be the first bit of the desired pattern -- for example, 1 1 0010 -- while a return to state a implies that this second bit is of no value in recognition and that the device must look for a 1 in the third bit). At this point the state diagram has been developed to three stages:



Following similar reasoning, the complete state diagram is this:



Thus the Pattern Detector requires 5 distinct states to recognize the desired pattern, and a transition from e to a indicates the desired pattern has occurred. The latter transition must be sensed and its occurrence transmitted to the Output Generator, as signal Y.

States are implemented with storage elements; that is, the device must "remember" which state it is in. Three binary storage elements are required to represent the five states. One storage element can represent only 2 states, 2 elements can represent 4 states, and 3 elements can exist in 8 different combinations. Eight states are more than enough, but 4 are too few; therefore, 3 elements are required. (The number of possible states always equals 2^n where n is the number of storage elements). In this example, simple clocked R-S flip-flops will be used as storage elements. The equations that result will contain all necessary logical conditions. Some of the terms may drop out during implementation because the T Series flip-flop is logically more powerful than a simple R-S, having the set-overrides-reset feature.

The third step is to assign a definite on-off configuration of the flip-flops to each network state. There is at present no known way to predetermine the assignments which lead to the most simple logic; however, a straightforward method is to simply assign them in binary sequence. Construct a truth table which shows the assignment of network states (a, b, c, d, e) to flip-flop on-off configurations. (Call the flip-flops FFA, FFB, FFC).

Network State	Corresponding Flip-Flop States		
	FFA	FFB	FFC
a	0	0	0
b	0	0	1
c	0	1	0
d	0	1	1
e	1	0	0
(no others required)			

A verbal interpretation of this truth table is: "if FFA, FFB, and FFC are all reset, then the network is in state a. If FFA and FFB are reset while FFC is set, then the network is in state b; etc."

The fourth step is derivation of a set of application equations which express in Boolean algebra the necessary relationships between the input signal, X, and the flip-flop configurations. This operation in effect translates the state diagram into Boolean algebra. It is done by comparing the state diagram step by step with the truth table above, and constructing a transition table as shown below. (For the moment ignore the circles around the 1's and 0's).

If initial state is:				And if X input is:	Then next state must be:			
Network	FFA	FFB	FFC		Network	FFA	FFB	FFC
a	0	0	0	0	a	0	0	0
a	0	0	0	1	b	0	0	1
b	0	0	1	0	c	0	1	0
b	0	0	1	1	b	0	0	1
c	0	1	0	0	d	0	1	1
c	0	1	0	1	b	0	0	1
d	0	1	1	0	a	0	0	0
d	0	1	1	1	e	1	0	0
e	1	0	0	0	a	0	0	0
e	1	0	0	1	b	0	0	1
(f)	1	0	1	illegal configurations (not used)				
(g)	1	1	0					
(h)	1	1	1					

Next, decide what conditions are required to make each flip-flop individually change state. First circle each change of state. For example in row 1 where state a goes to state a, no flip-flop changes, therefore no action is required. On the other hand, in row 2 where a goes to b (FFA, FFB, FFC are 0, 0, 0 and change to 0, 0, 1), FFC does change state (reset to set). Now write the input equations to each flip-flop. (For convenience drop the FF designations and call the flip-flops A, B, C). For instance, in the FFA column, there are three changes, all in the last three rows. In row 8, FFA must be set whenever the input is 1 (X is true) and the initial flip-flop configuration is 011 (also written as $\bar{A}BC$). Thus $s_A = X(\bar{A}BC)$, which means set A when X ($\bar{A}BC$) is True. Row 9 shows that A must be reset whenever input X is 0, and the flip-flops are 100; thus $r_A = \bar{X}(A\bar{B}\bar{C})$. The last row shows that A must be reset when the network goes from state e to state b; thus $r_A = X(A\bar{B}\bar{C})$. The equations can be summarized:

$$s_A = X\bar{A}BC$$

$$\text{and } r_A = \bar{X}A\bar{B}\bar{C} + XA\bar{B}\bar{C}$$

Similarly,

$$s_B = \bar{X}\bar{A}\bar{B}C$$

$$r_B = X\bar{A}B\bar{C} + \bar{X}\bar{A}BC + X\bar{A}BC$$

$$s_C = X\bar{A}\bar{B}\bar{C} + \bar{X}\bar{A}B\bar{C} + X\bar{A}B\bar{C} + XA\bar{B}\bar{C}$$

$$r_C = \bar{X}\bar{A}\bar{B}C + \bar{X}\bar{A}BC + X\bar{A}BC$$

The mechanization of these equations with hardware results in a network which will properly assume the states depicted in the state diagram. However, a simpler network may be constructed to do the same, with a consequent hardware saving. The process of finding the equivalent but simpler network is called logical simplification. There is no one technique that will always force the simplest solution, but a number of techniques are available for different cases, as described in the literature.* Thus simplification is an art rather than a science, and the results depend largely on the skill of the logician.

One simplification is elimination of restrictions that provide for contingencies which will never occur. It often happens, as in this example, that more flip-flop configurations are available than are used. The unused states are called illegal states, because the network is so designed that it bypasses those states. In the present example, these are shown in the transition table as states f ($A\bar{B}C$), g ($A\bar{B}\bar{C}$), and h ($AB\bar{C}$). Since these never occur, some of the configurations which do occur can be uniquely represented with fewer variables than three. For instance, it is sufficient to specify $\bar{B}C$ rather than $\bar{A}\bar{B}C$ for state b, since $\bar{A}\bar{B}C$ never occurs, and therefore $\bar{B}C$ by itself represents a unique condition. Applying this reasoning, the following terms may be simplified as shown:

$\bar{A}\bar{B}C$ can be replaced by $\bar{B}C$ (state b)
 $\bar{A}B\bar{C}$ can be replaced by $B\bar{C}$ (state c)
 $\bar{A}BC$ can be replaced by BC (state d)
 $A\bar{B}\bar{C}$ can be replaced by A (state e)

When the terms above are substituted in the original group of equations, these equivalents are obtained:

$$s_A = XBC$$

$$r_A = \bar{X}A + XA$$

$$s_B = \bar{X}\bar{B}C$$

$$r_B = XB\bar{C} + \bar{X}BC + XBC$$

$$s_C = X\bar{A}\bar{B}\bar{C} + \bar{X}B\bar{C} + B\bar{C} + XA\bar{B}\bar{C}$$

$$r_C = \bar{X}\bar{B}C + \bar{X}BC + XBC$$

Certain equalities are always true in Boolean algebra, as expressed by the theorems on page 31. These lead to further simplification:

$$s_A = \boxed{XBC}$$

$$r_A = A(\bar{X} + X) = \boxed{A}$$

$$s_B = \boxed{\bar{X}\bar{B}C}$$

$$r_B = XB\bar{C} + BC(\bar{X} + X) = B(X\bar{C} + C) = \boxed{BX + BC}$$

$$s_C = X\bar{B}\bar{C}(A + \bar{A}) + B\bar{C}(X + \bar{X}) = \bar{C}(X\bar{B} + B) = \boxed{\bar{C}X + \bar{C}B}$$

$$r_C = BC(X + \bar{X}) + \bar{X}BC = C(B + \bar{X}\bar{B}) = \boxed{CB + C\bar{X}}$$

Last, derive the output (Y) equation. The state diagram indicates that Y must be made True when the network goes from state e to state a. The transition table shows this in row 9 (next to last row), and shows that the only flip-flop change in this transition occurs at the reset A input. The equation for this change is thus $Y = \bar{X}A\bar{B}\bar{C}$. This can be simplified to $Y = XA$, because the conditions $A\bar{B}C$ and $A\bar{B}\bar{C}$ are illegal.

MECHANIZING THE PATTERN DETECTOR

This crucial step determines hardware cost. Its outcome depends on the variety and cost of electronic logic elements available to the logic designer. The most economical result, in terms of both design time and hardware, is obtained when low cost electronic devices may be directly substituted for the simplest equation terms. Otherwise additional equation manipulation is required, and often additional logic elements are also required if the equations must be made more complex to satisfy hardware availability. This is particularly true in the case when the designer is restricted exclusively to one logic function such as NAND or NOR, as explained on pages 3, 4 and 5 in Section I.

With T Series natural logic, implementation is simple:

1. When the equations have been reduced to simplest form, substitute AND, OR, NAND, or NOR gates by direct inspection (use table on page 11 or logic diagrams in Section II).

- Inspect to see if hardware can be further reduced by forming logic functions at buffer, inverter, or flip-flop outputs (see page 12).
- Eliminate gates and wiring where possible by using the T Series flip-flop set-overrides-reset feature (see page 9). Leave flip-flop inputs open for wired True, or ground for wired False.
- Decide which flip-flop module type is to be used, and determine whether built-in gating structures are available at flip-flop inputs. Some logic elements external to the flip-flop module may be eliminated in this way.
- Establish logic to reset the network to the initial state (state a) when desired.
- Check the loading on each output to verify conformance to load restrictions (page 12). With the high fan-out of 14 this generally presents no problem, unless very high speeds or long lines are needed. However, if overload exists, add buffers or inverters where required.
- The remaining consideration is that of system speed (see page 7). This depends partly on wiring lengths, and therefore the physical layout of modules in racks must be determined. Wiring rules are given on page 12.
- Ground each unused input of an OR or NOR gate to give a wired False signal. Also ground mark and erase inputs if not used.
- Leave all unused AND inputs open to give wired True signal.

Now implement the unit using these rules, starting with rules 1, 2, and 3. Inspection of $s_A = X B C$ shows that a 3-input AND is needed at the set $\bar{A}$ input. Equation $r_A = A$ can be replaced with $r_A = 1$ because the set input when True overrides the reset input, giving the same logical result. (This is apparent upon examination of the transition table, which shows, in column 7, that FFA may be allowed to reset on any transition except d to e). Equation $s_B = \bar{X} \bar{B} C$ calls for a 3-input AND. Note that $\bar{X}$ is not available directly, but must be created with an inverter. Equation $r_B = B X + B C$ calls for an AND/OR. Inspection of $s_C = \bar{C} (X + B)$ indicates a 2-input OR is required, ANDed with $\bar{C}$. Finally, $r_C = C B + C \bar{X}$ requires another AND/OR.

Assume the FT10 module will be used. In this module, all set inputs have a built-in 2-input AND. Applying rule 4 allows use of 2-input ANDs for 3-input ANDs on the set inputs.

Rule 5 requires that logic be established to reset the flip-flops. This is best accomplished at the erase inputs with

a normally closed switch to ground, as shown on p. 39.

Application of rule 6 shows that no logic line is loaded with more than 5 loads, therefore as many as two line terminators may be used if needed to decrease delay to a minimum (no more than 1 per branch).

If the delay through the X-to- $\bar{X}$ inverter is troublesome, the input equations for s_B , r_B , and Y can be rewritten to replace $\bar{X}$ with X: $s_B = \bar{X} \bar{B} C = X + B + \bar{C}$, $r_B = \bar{X} B \bar{C} = X + \bar{B} + C$, and $Y = \bar{X} A = X + \bar{A}$. However, this requires the substitution of different gates.

Rules 8 and 9 are applied after the logic element module is chosen, which should be done last.

The Logic Diagram in its final form is shown on page 45.

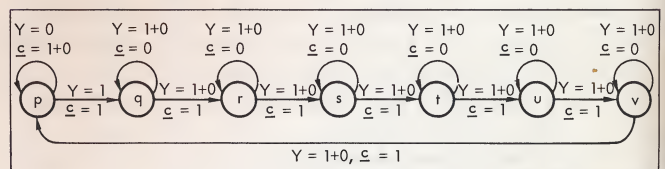
DESIGNING THE OUTPUT SIGNAL GENERATOR

Stated in words, the problem is: 1. generate specified output signals on two lines, with the leading edge of the first level change starting on the clock pulse that immediately follows the appearance of the condition $Y = 1$; and 2. inhibit the start of another output cycle until 700 nanoseconds have elapsed from the start of the first one.

Since a series of precisely timed signals must be generated, and since the output pulsewidths are all integral multiples of the clock pulse period, the clock pulse can be used as a convenient signal source to generate the output. The problem may now be restated: design a logic network that counts clock pulses starting with the first clock pulse following the leading edge of $Y = 1$; that generates outputs as specified; and that ignores subsequent change in Y for a period of 700 nsec. after the start of an output cycle.

In this case there are two input signals. One is Y, which has the form 00000100000... (that is, Y remains at 0 until pattern is recognized, then returns to 0 until next pattern, etc.). The other, designated $\underline{c}$ (the clock pulse used as signal input), has the form 01010101...

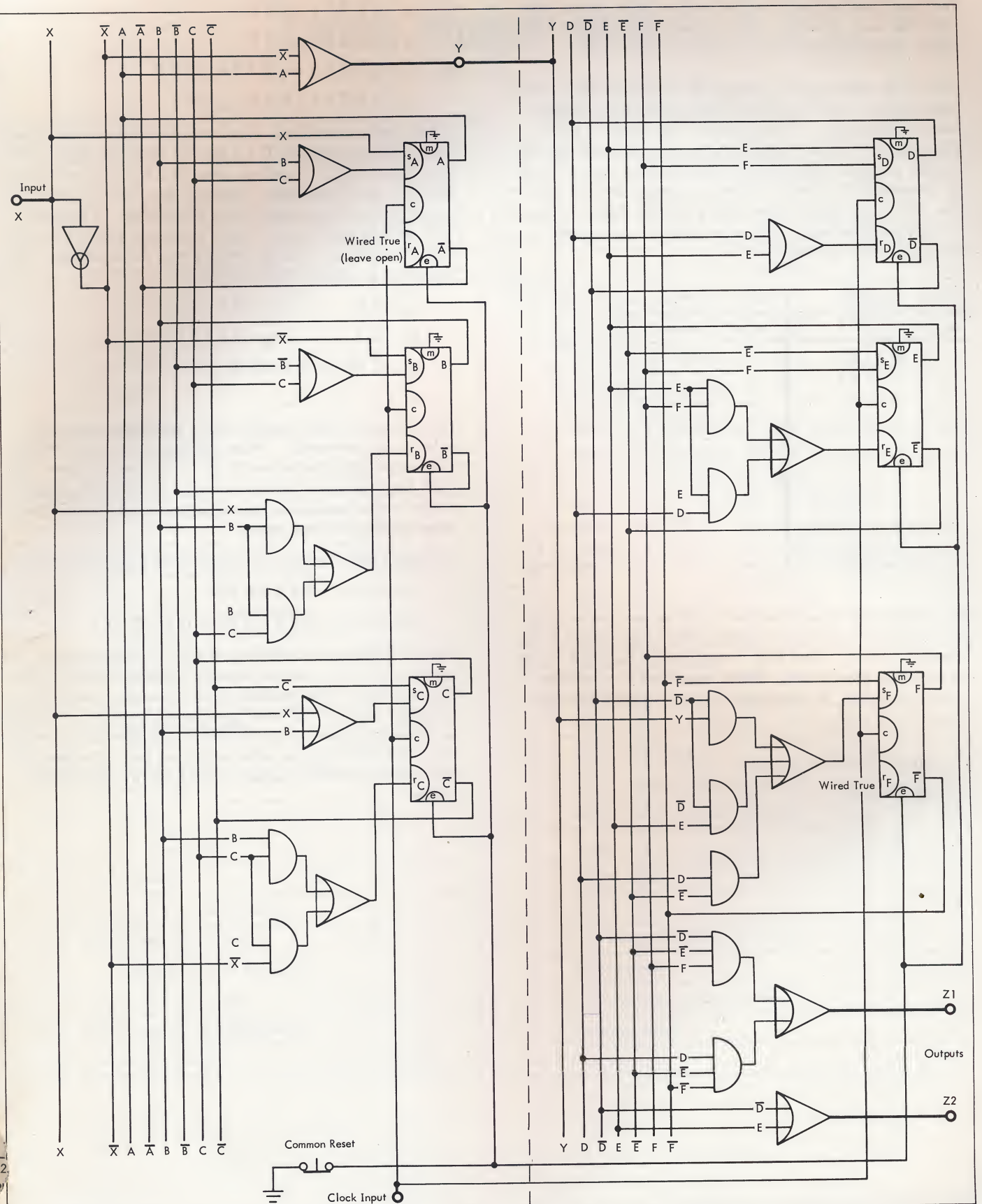
First, draw a state diagram, as in the previous problem. Since the total output cycle time is 700 nsec., 7 counts of $\underline{c}$ are required.



The output equations can now be written in terms of the network states:

$$Z1 = q + t$$

$$Z2 = \bar{t} + u$$



LOGIC DIAGRAM, PATTERN DETECTOR

LOGIC DIAGRAM, OUTPUT SIGNAL GENERATOR

The specification that a second output cycle cannot start until 700 nsec. after the first one begins is satisfied by simply ignoring any change in Y for 7 counts of $\underline{c}$.

Now set up the state assignment and transition table. Arbitrarily assign states in straight binary sequence as before. Seven states require 3 flip-flops ($2^3 = 8$) which are here designated D, E, and F. Each state could be examined for all four combinations of the two independent inputs Y and $\underline{c}$. However, $\underline{c} = 0$ never causes a change, and the condition of Y is immaterial from state p through state v; therefore the rows having $\underline{c} = 0$ can be omitted, and except in state p, Y may be written 1 + 0.

Initial Network State	Assigned Flip-Flop States	Inputs Y $\underline{c}$	Next Network State	Corresponding Next Flip-Flop States	
	$\underline{D}$ $\underline{E}$ $\underline{F}$			$\underline{D}$ $\underline{E}$ $\underline{F}$	
p	0 0 0	0 1	p	0 0 0	No change
p	0 0 0	1 1	q	0 0 ①	Change F
q	0 0 1	1+0 1	r	0 ① ①	Change E, F
r	0 1 0	1+0 1	s	0 1 ①	Change F
s	0 1 1	1+0 1	t	① ① ①	Change D, E, F
t	1 0 0	1+0 1	u	1 0 ①	Change F
u	1 0 1	1+0 1	v	1 ① ①	Change E, F
v	1 1 0	1+0 1	p	① ① 0	Change D, E
w	1 1 1				illegal state

Now derive the input equations from the table by writing the conditions required to perform all changes noted in the remarks column. Note that Y need not be included except in changing from p to q. (If the equations were written with Y included, it would drop out during simplification since $Y + \bar{Y} = 1$).

$$1. \quad s_D = \underline{c} \bar{D} E F$$

$$r_D = \underline{c} D E \bar{F}$$

$$2. \quad s_E = \underline{c} \bar{D} \bar{E} F + \underline{c} D \bar{E} \bar{F}$$

$$r_E = \underline{c} \bar{D} E F + \underline{c} D E \bar{F}$$

$$3. \quad s_F = \underline{c} \bar{D} \bar{E} \bar{F} Y + \underline{c} \bar{D} E \bar{F} + \underline{c} D E \bar{F}$$

$$r_F = \underline{c} \bar{D} \bar{E} F + \underline{c} \bar{D} E F + \underline{c} D E F$$

These can be simplified. First note that $D E F$ is an illegal configuration; therefore $\bar{D} E F$ may be replaced by $E F$ in the equations for s_D , r_E , and r_F ; also, $D E \bar{F}$ can be replaced by $D E$ in the r_D equation. Second, note that the clock signal $\underline{c}$, when connected to the clock input, is ANDed with set and reset terms by logic contained within the flip-flop. Therefore it may be omitted from the equations. The equations in reduced form are now:

$$s_D = E F$$

$$s_E = \bar{E} F$$

$$r_D = D E$$

$$r_E = E F + E D$$

$$s_F = \bar{F} (\bar{D} Y + \bar{D} E + D \bar{E})$$

$$r_F = F$$

Now implement the flip-flop input equations, using the rules given previously. Note that the set-overrides-reset feature permits elimination of $r_F = F$ because r_F wired True (left open) provides the same result. A reduction of gate inputs is also possible at s_E and s_F because FT10 flip-flops have built-in 2-input gates.

To obtain the Z outputs, implement the output equations:

$$Z1 = q + t = \bar{D} \bar{E} F + D \bar{E} \bar{F}$$

$$Z2 = \bar{r} + \bar{u} = \bar{D} \bar{E} \bar{F} + D \bar{E} F = \bar{D} \bar{E} = \bar{D} + E$$

The entire device, consisting of six flip-flops together with gating structures, can be directly implemented with components from 1 FT10 module, 1 LT10 module, and 1 LT12 module. Only 11 buffered gates and 1 inverter are required with natural logic. A pure NAND implementation, using the same flip-flops and also permitting logic functions to be formed at NAND outputs, would require 25 NAND gates!

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IT10

IT11

* Add \$2
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Model	Description	Ckts. per Module	Price	Model	Description	Ckts. per Module	Price
AT10	Cable receivers	14	\$140	IT13	4 x 4 inverted AND matrix (NAND matrix)	1	\$100
AT11	Cable receivers/drivers	14	260	IT18	Inverted ANDs (NANDs)	10	70
AT12	Cable drivers	14	140	LT10	Logic elements (ANDs, ORs, NANDs)	12	72
AT14	T Series to +8v interface cable drivers	7	105	LT11	Logic elements (AND/ORs, AND/NORs)	4	72
AT15	+8v to T Series interface cable receivers	18	79	MT10	Fixed mount 32-module case, solder-tail	-	220
AT22	Schmitt triggers	2	80	MT12	Fixed mount 32-module case, wire-wrap	-	220
BT10	Buffered AND/OR gates	8	68	MT30	Hinge mount 32-module case, solder-tail	-	240
BT11	Buffered ANDs	12	80	MT32	Hinge mount 32-module case, wire-wrap	-	240
BT12	Binary decoders	2	97	MTD-1	Drawer type 90-module case, solder-tail	-	700
BT13	4 x 4 buffered AND matrix	1	100	MTD-2	Drawer type 90-module case, wire-wrap	-	700
BT18	Buffered ANDs	10	70	NT10	+8v interface, 4 x 4 buffered AND matrix	1	100
CT10	High frequency clock oscillator (1 Mc to 10 Mc)	1	72*	NT11	+8v interface, 4 x 4 NAND matrix	1	100
CT16	Medium frequency clock oscillator (7.8 Kc to 2 Mc)	1	100*	NT17	T Series to negative logic interface (ANDs)	8	55
DT12-1	4-bit D/A converters with buffers and ref.	2	85	NT18	Negative logic to T Series interface (ANDs)	8	55
DT12-2	4-bit D/A converters	2	55	OT17	Adjustable one-shots (100 nsec to 100 µsec)	4	105
DT13-1	6-bit D/A converters with buffers and ref.	2	95	PT10	Compact power supply	-	280
DT13-2	6-bit D/A converters	2	75	PT12	High output power supply	-	980
ET10-XX	14 conductor cable with connectors	-	40±2/ft**	QT14	Lamp drivers	12	100
ET11	Front-edge cable connectors	-	5	RT14	Relay drivers	12	100
ET12-XX	14 conductor cable	-	2/ft	VT10	Jumper kit (500 wires)	-	75
ET13	Cable dummy load	-	15	VT11	Individual module connector, wire-wrap	-	5
FT10	Basic flip-flops	6	92	VT12	Individual module connector, solder-tail	-	5
FT11	4-bit high speed counter	1	76	XT10	Terminators	48	30
FT12	Gated flip-flops	8	118	ZT10	Extender module	-	40
FT19	4-bit multipurpose counters/registers	2	140	ZT11	Blank module	-	20
FT20	8-bit buffered latch registers	2	100	ZT15	Cable plug module (solder connections)	-	30
FT26	4 x 8 buffered latch matrix (OR inputs)	1	80	ZT20	Blower assembly	-	80
FT27	Buffered latches (OR inputs)	12	99	ZT23	Cable plug module (pressure contacts)	-	25
IT10	Inverted AND/OR gates (AND/NORs)	8	68	ZT37	Breadboard module	-	20
IT11	Inverted ANDs (NANDs)	12	80	ZT39	Lamp and socket	-	1.50

* Add \$25 for each crystal. Specify frequency.
** 40 for basic assembly + \$2 per foot of cable.
See reverse side for discount schedule.

MODULE DISCOUNT POLICY

SDS grants single-order discounts on purchases of T Series modules and accessories based on the following schedule.

Order Exceeding	Discount	Order Exceeding	Discount
\$ 5,000	3%	\$30,000	10%
10,000	5%	50,000	13%
20,000	7%		

A single order is defined as one purchase order placed and not subsequently altered in any manner by one customer specifying delivery and billing to single addresses.

SDS SALES OFFICES

EXECUTIVE OFFICES

1649 Seventeenth Street
Santa Monica, Calif. 90404
(213) 871-0960

* INSTRUMENTS DEPT.

555 So. Aviation Blvd.
El Segundo, Calif. 90245
(213) 679-4511

EASTERN

* Maryland Engineering Center
12150 Parklawn Drive
Rockville, Md. 20852
(301) 933-5900

69 Hickory Drive
Waltham, Mass. 02154
(617) 899-4700

1301 Avenue of the Americas
New York City, N. Y. 10019
(212) 765-1230

12 Huntington Brook
Rochester, N. Y.
(716) LU6-1500

One Bala Avenue Building
Bala-Cynwyd, Pa.
(215) 667-4944

* Brogan Associates, Inc.
Representatives
80 Urban Avenue
Westbury, L. I., N. Y. 11590
(516) 333-6683

* Brogan Associates, Inc.
Representatives
69 Hickory Drive
Waltham, Mass. 02154
(617) 894-3250

* Brogan Associates, Inc.
Representatives
780 N. River View Drive
Totowa, N. J. 07512
(201) 256-0174

* Brogan Associates, Inc.
Representatives
107 West Ridge Pike
Conshohocken, Pa. 19428
(215) 825-0510

* Brogan Associates, Inc.
Representatives
474 Thurston Road
Rochester, N. Y.
(716) FA8-2350

* Brogan Associates, Inc.
Representatives
202 Arterial Road
Syracuse, N. Y. 13206
(315) 437-2988

SOUTHERN

Holiday Office Center
3322 South Memorial Pkwy.
Huntsville, Alabama
(205) 881-5746

Suite 111, Washington Plaza
Parker Dr. & U.S. Hwy. #1
Titusville, Florida
(305) 267-6181

2732 Gallinghouse
New Orleans, La. 70114
(504) 367-7439

6434 Maple Avenue
Dallas, Texas 75235
(214) 357-0451

* 3334 Richmond Avenue
Houston, Texas 77006
(713) 526-2693

MIDWEST

* 3150 Des Plaines Avenue
Des Plaines, Ill. 60018
(312) 824-8147

* 17500 W. Eight Mile Road
Southfield, Mich. 48076
(313) 353-7360

Suite 222, Kimberly Bldg.
2510 South Brentwood Blvd.
St. Louis, Mo. 63144
(314) 968-0250

One Parkway Center
875 Greentree Road
Pittsburgh, Pa. 15220
(412) 921-3640

WESTERN

* 1360 So. Anaheim Blvd.
Anaheim, Calif. 92805
(213) 865-5293 (F.X.)
(714) 774-0461 (Local)

* 2526 Broadway Avenue
Santa Monica, Calif. 90404
(213) 870-5862

* Sunnyvale Office Center
505 West Olive Avenue
Sunnyvale, Calif. 95128
(408) 736-9193

Fountain Professional Bldg.
9000 Manual Blvd. N. E.
Albuquerque, N. M. 87112
(505) 298-7683

Suite 501
Dravo Building
225 108th Street N. E.
Bellevue, Wash. 98004
(206) 454-3991

* Showalter-Judd, Inc.
Representatives
1806 So. Bush Place
Seattle, Wash. 98144
(206) EA 4-7911

CANADA

864 Lady Ellen Place
Ottawa 3, Ontario
(613) 722-3242

INTERNATIONAL REPRESENTATIVES

ENGLAND

GEC Computers
& Automation Ltd.
East Lane, Wembley
Middlesex, England

FRANCE

Compagnie Europeenne
d'Automatisme Electronique

EXECUTIVE OFFICES

101 Boulevard Murat
Paris 16^{eme}, France

SALES OFFICE

17 Rue de la Reine
Boulogne 92, France

JAPAN

F. Kanematsu & Co. Inc.
Central P. O. Box 141
New Kaijo Building
Marunouchi
Tokyo, Japan

* Module and Instrument Applications staff is located at these offices.

Scientific Data Systems

1649 Seventeenth Street

Santa Monica, California 90404

Telephones: 213/871-0960

and 213/451-4747



September 27, 1966

To Those Interested
in High-Quality,
Integrated Circuit,
General System Modules

Dear Sir:

Thank you for your interest in T Series integrated circuit logic modules. The enclosed catalog is a brand new revision and includes several recent additions to the product line.

The catalog is divided into three sections. The first presents basic specifications of the T Series line and includes an informative discussion on design requirements common to all digital systems. The second section contains data on each module in the T Series family, the integrated circuits, and hardware accessories. The closing section is a primer on logic design and includes a detailed example for you to work through. A product index appears on the inside back cover. We hope you find this catalog useful and informative.

If you would like further assistance please contact me directly or call your nearest SDS sales office or representative. Addresses are listed on the back cover of the brochure. Module specialists are located in these offices:

El Segundo, California

Santa Monica (Broadway), California

Anaheim, California

Sunnyvale, California

Seattle, Wash. (Showalter-Judd)

Houston, Texas

Des Plaines, Illinois

Southfield, Michigan

New England (Brogan Assoc.)

Rockville, Maryland

Sincerely,

A handwritten signature in dark ink, appearing to read 'R.D. Alexander', with a stylized flourish at the end.

Richard D. Alexander
Manager, Instruments Marketing

Enclosure